# Intrinsic Parameter Fluctuations in Conventional MOSFETs at the scaling Limit: A Statistical Study

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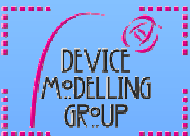

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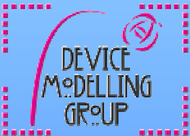
- Introduction
- Methodology
  - Calibration
  - Scaling
  - Atomistic Simulation
- Results
- Conclusions



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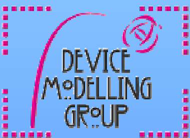


# The road map requirements

ITRS 2003

Near-Term TN characteristics

| Year of Production | 2003 | **2004** | 2005 | 2006 | **2007** | 2008 | 2009 |
|---|---|---|---|---|---|---|---|
| **Technology Node** | | **hp90** | | | **hp65** | | |
| DRAM *½ Pitch (nm)* | 100 | 90 | 80 | 70 | 65 | 57 | 50 |
| MPU/ASIC M1 *½ Pitch (nm)* | 120 | 107 | 95 | 85 | 75 | 67 | 60 |
| MPU/ASIC *Poli Si ½ Pitch (nm)* | 100 | 90 | 80 | 70 | 65 | 57 | 50 |
| MPU *Printed Gate length (nm)* | 65 | 53 | 45 | 40 | 35 | 32 | 28 |
| MPU *Physical Gate Length (nm)* | 45 | 37 | 32 | 28 | 25 | 22 | 20 |

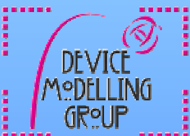
Long-Term TN characteristics

| Year of Production | **2010** | 2012 | **2013** | 2015 | **2016** | **2018** |
|---|---|---|---|---|---|---|
| **Technology Node** | **hp45** | | **hp32** | | **hp22** | |
| DRAM ½ Pitch (nm) | 45 | 35 | 32 | 25 | 22 | **18** |
| MPU/ASIC M1 *½ Pitch (nm)* | 54 | 42 | 38 | 30 | 27 | **21** |
| MPU/ASIC *Poli Si ½ Pitch (nm)* | 45 | 35 | 32 | 25 | 22 | **18** |
| Printed Gate Length (nm) | 25 | 20 | 18 | 14 | 13 | **10** |
| Physical Gate Length (nm) | 18 | 14 | 13 | 10 | 9 | **7** |

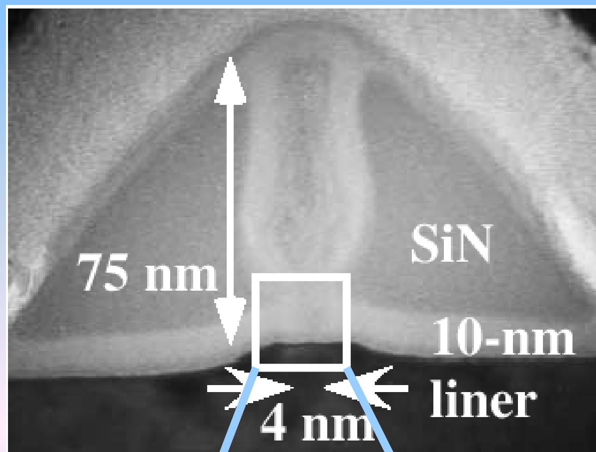
| Year of Production | **2019** | **2022** | **2025** |
|---|---|---|---|
| **Technology Node** | **15** | **10** | **7** |
| Printed Gate length | 9 | 6 | 4 |
| Physical Gate Length (nm) | 6 | 4 | 3 |

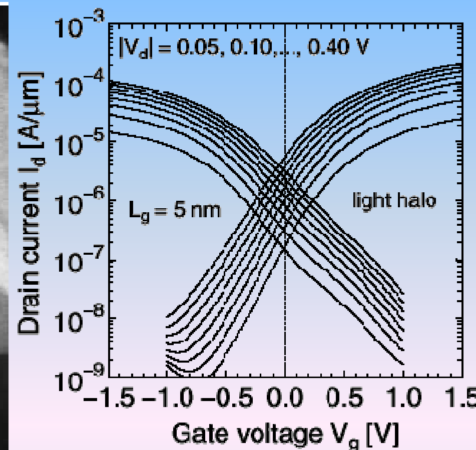
IBM roadmap

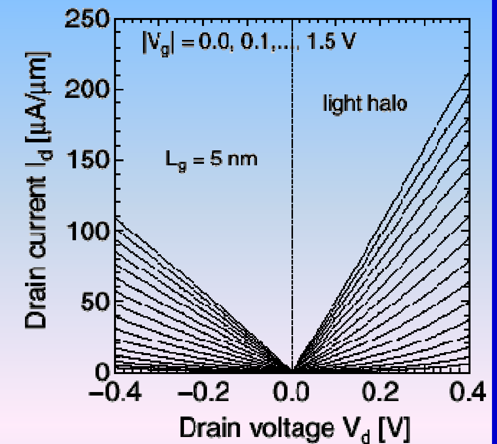
M. Ieong, NPMS/SIMD
Maui Dec. 2003



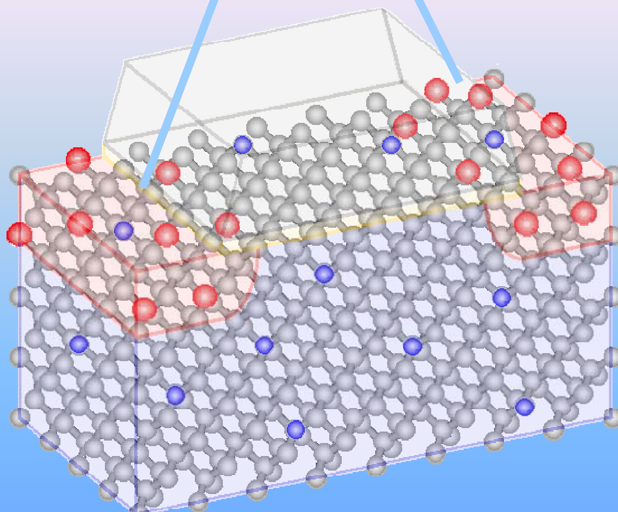
# When the number and position of dopants matter MOST!



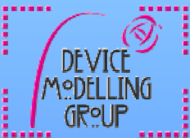




H. Wakabayashi et al. IEDM 03

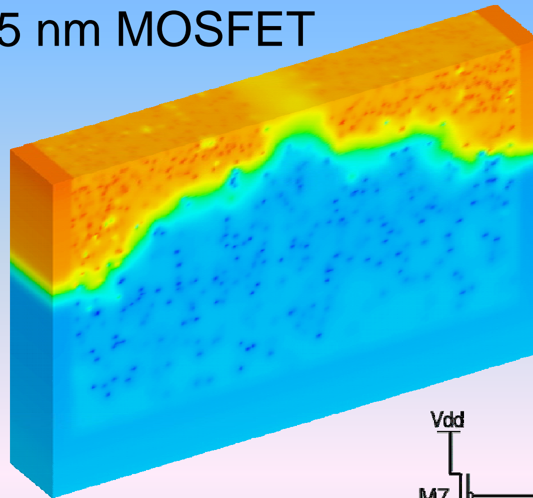


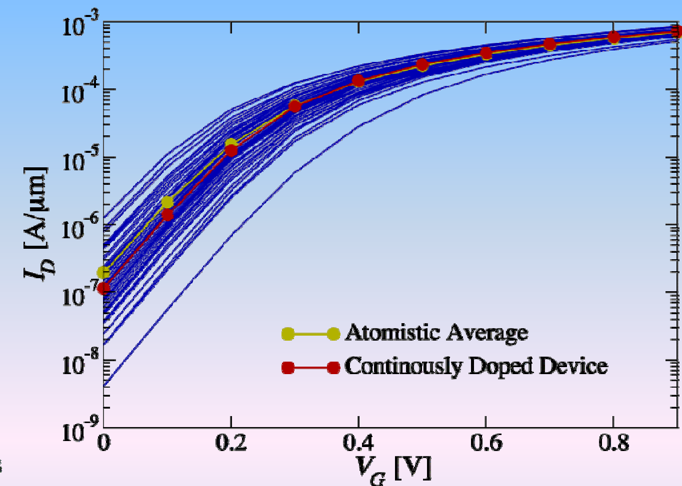
Atomistic device and process simulation is important to resolve the impact of each individual dopant in the device in terms of electrostatics and transport

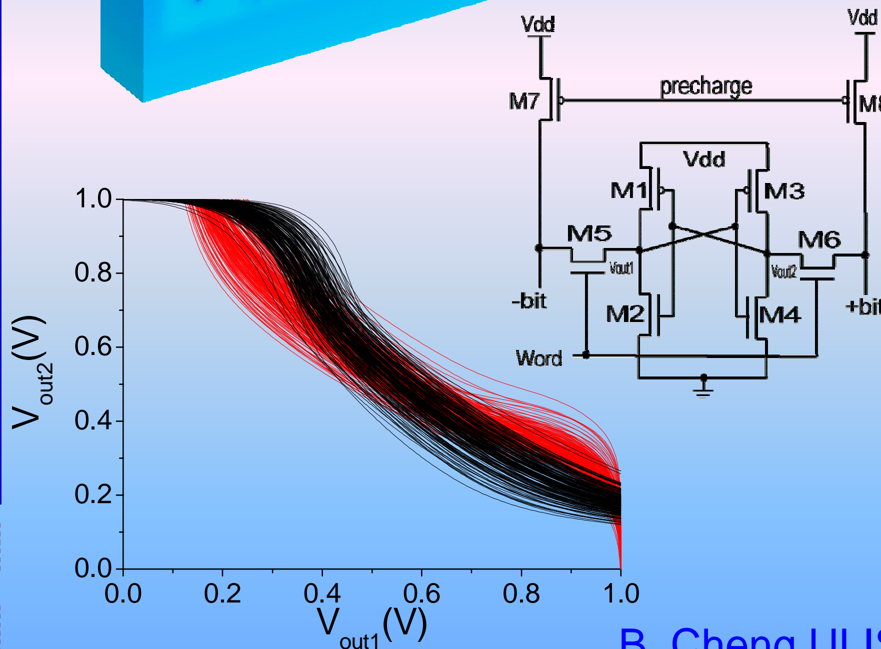


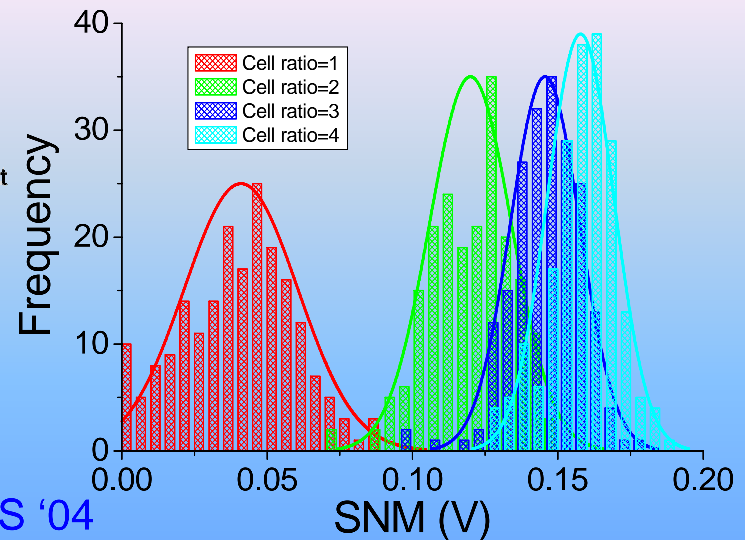
# Intrinsic parameter fluctuations already affect real circuit

35 nm MOSFET

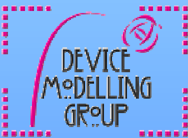





B. Cheng ULIS '04



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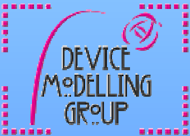
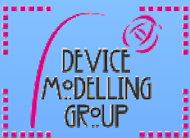


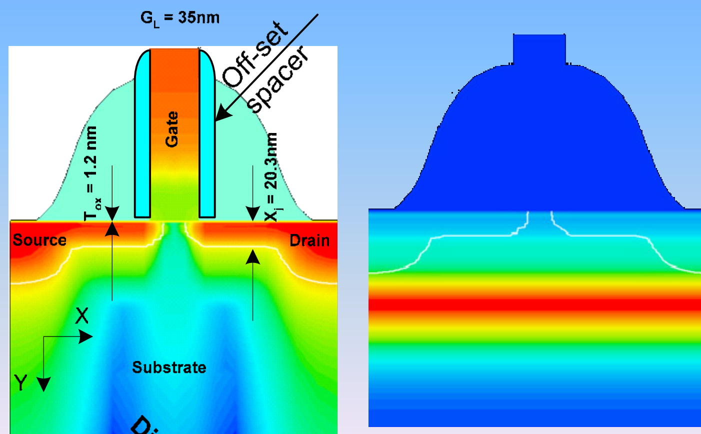
# Methodology I: *calibration*

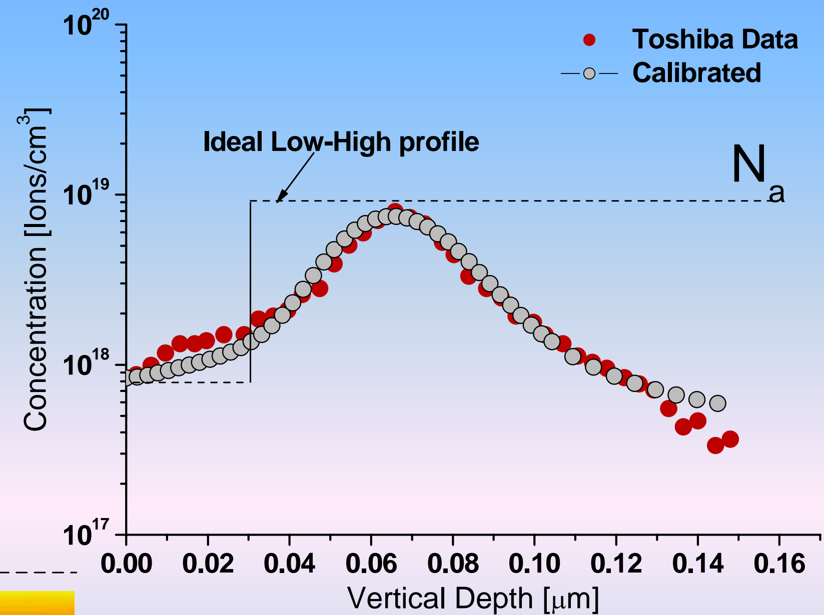
- The device simulations have been calibrated In respect of a real reference 35 nm MOSFET* used as a base for further scaling.
- Full process simulation was performed to obtain device structure and channel doping profiles of the 35n n-channel device.
- Device simulation was used in order to verify the structure and to extract the relevant transport parameters.

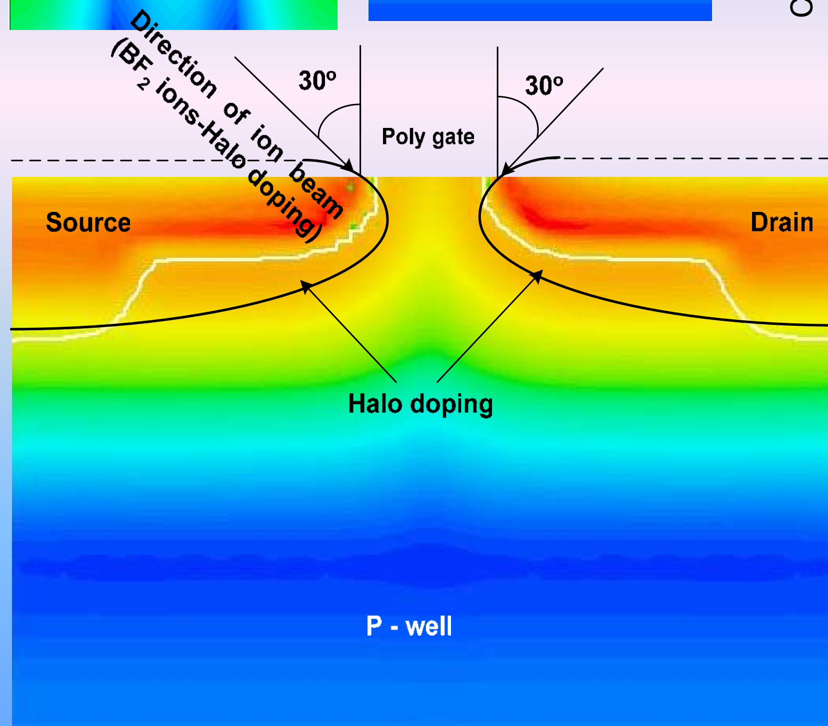



* S. Enaba, *et. al.*, IEDM '02

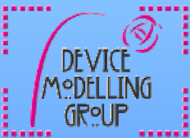
# The calibrated doping profiles



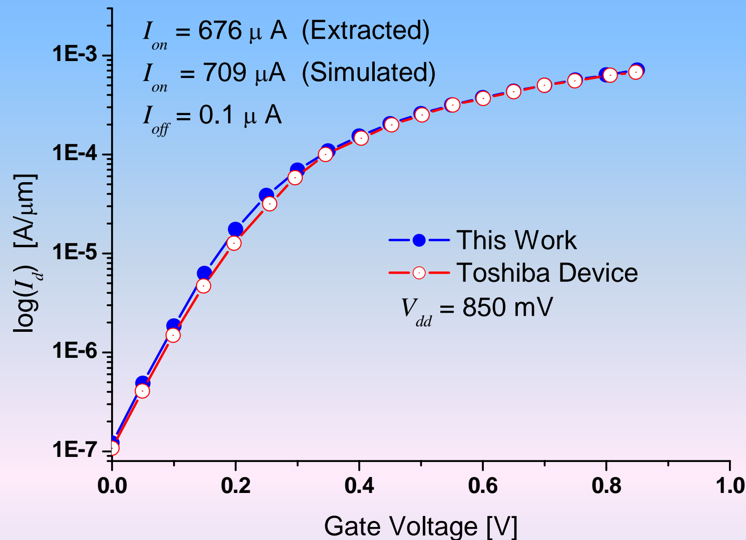



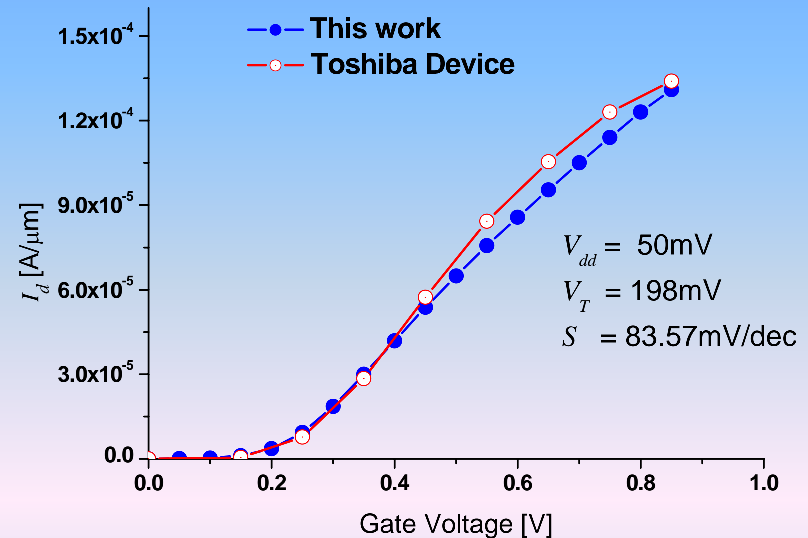



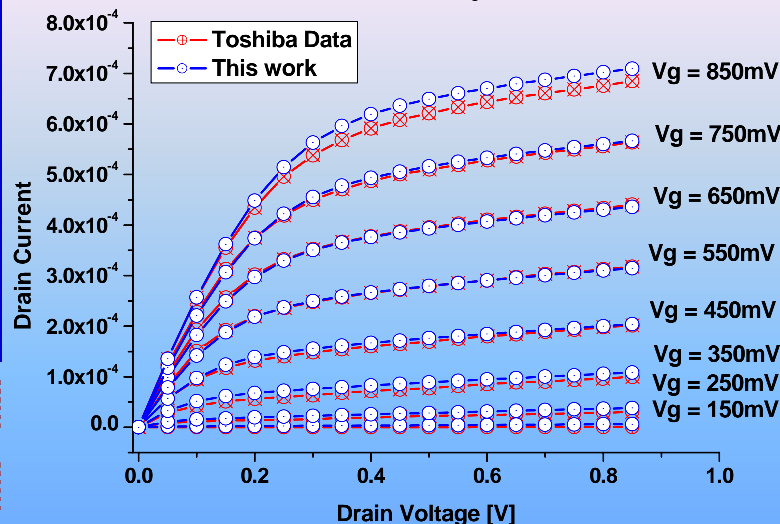

- The calibrated device structure,
- 1D channel doping profile and,
- Halo doping profile in the S/D extension region



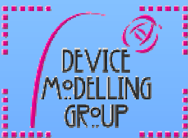
# The calibrated device characteristics




$I_d$-$V_g$ characteristics of the calibrated and the measured data of the 35nm device at high drain voltage $V_{dd}$ = .85V, at low drain voltage of $V_{dd}$ = 0.05V and the $I_d$-$V_d$ characteristics



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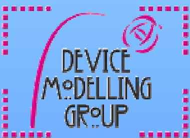
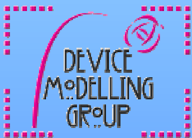


# Methodology II: *Scaling*

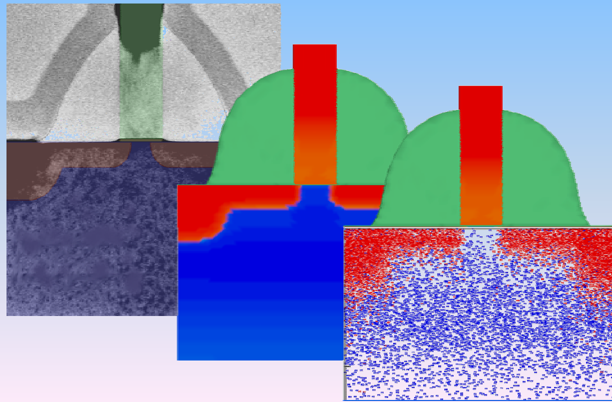
- The scaling strategy is based on the generalised scaling rules* and the ITRS roadmap predictions for high performance devices up to the year 2018
- The well calibrated 35 nm real MOSFET has been used as a base for further scaling of the **25, 18, 13** and **9** nm transistors (required for **65, 45, 32** and **22** nm technology nodes respectively)
- All the device structures are obtained from full process simulations on which the device simulation analyses have been performed

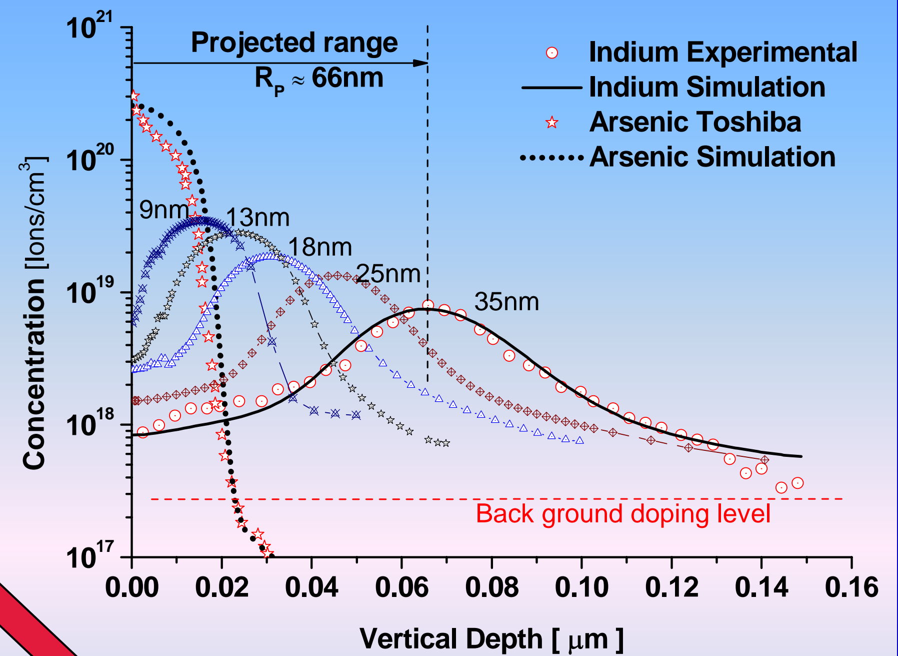


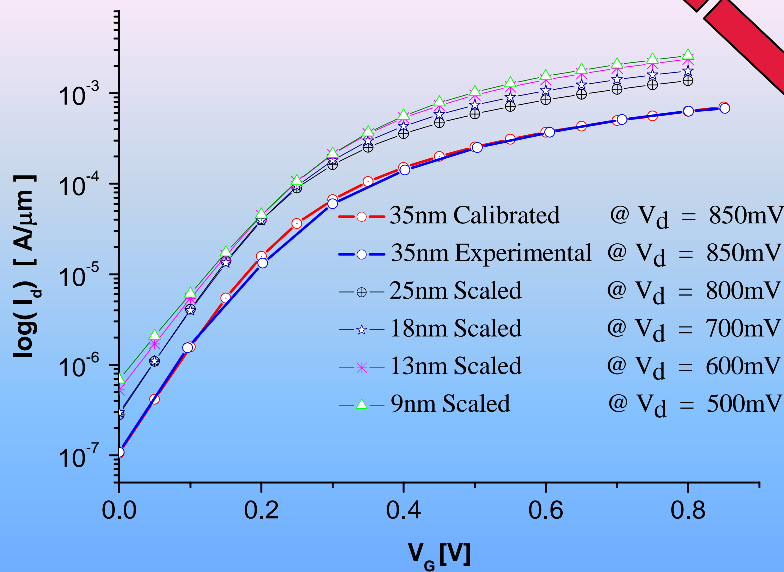

* G. Baccarani, *et. al*, 1984

# Scaling MOSFETs up to the end of ITRS

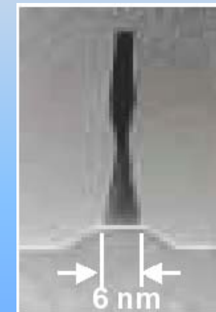
## 35 nm (Toshiba IEDM 02)

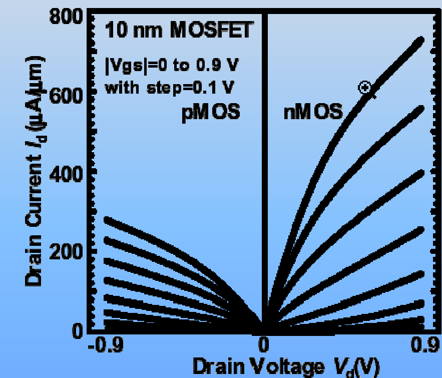


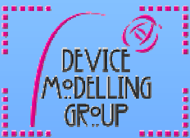



## 6nm nm (VLSI '04 )



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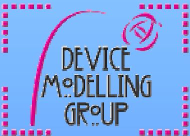
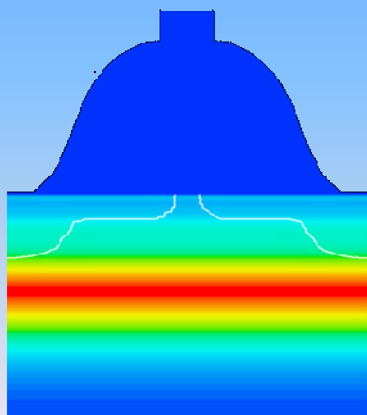
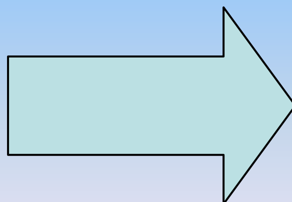
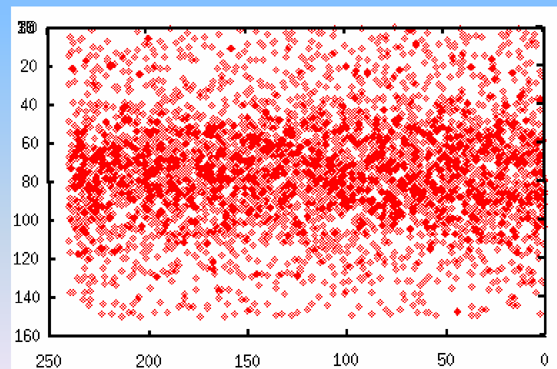
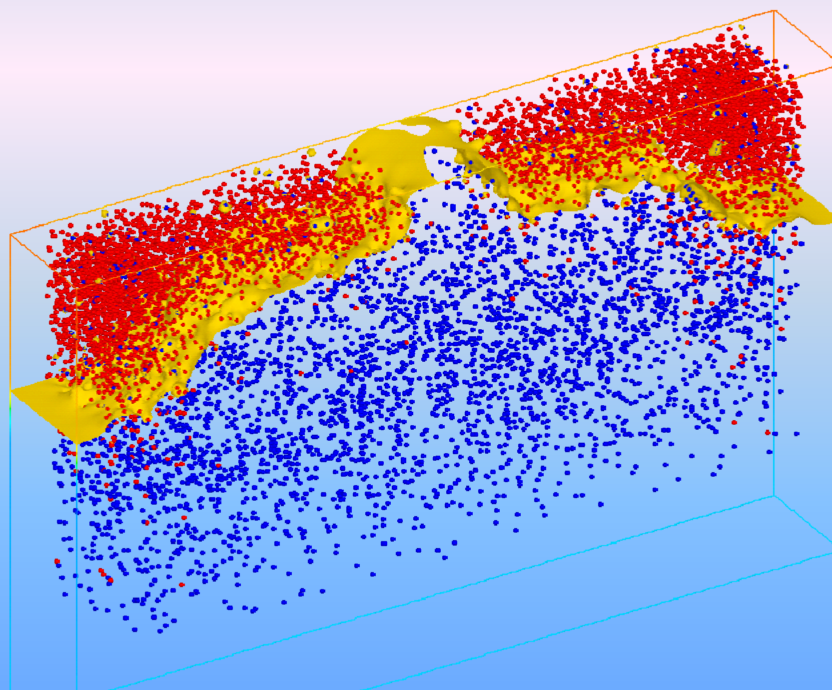


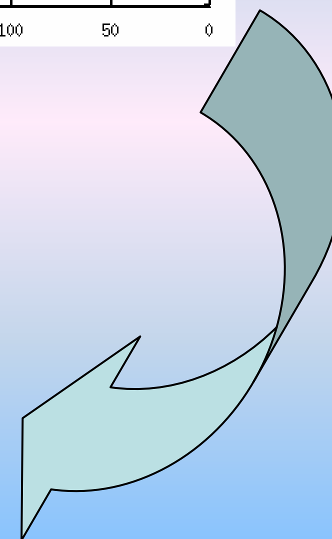
# From continuous doping to Atomistic

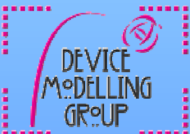




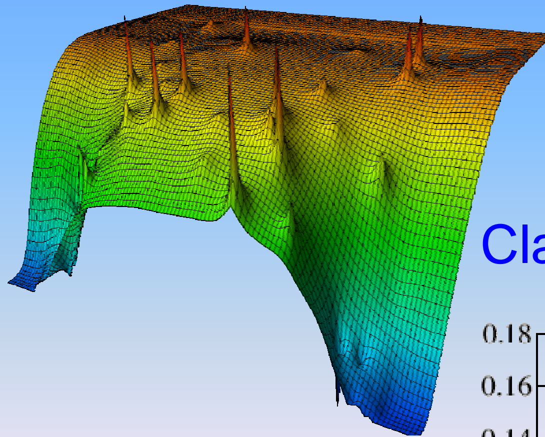




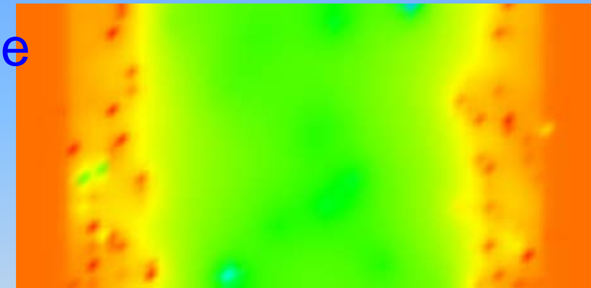


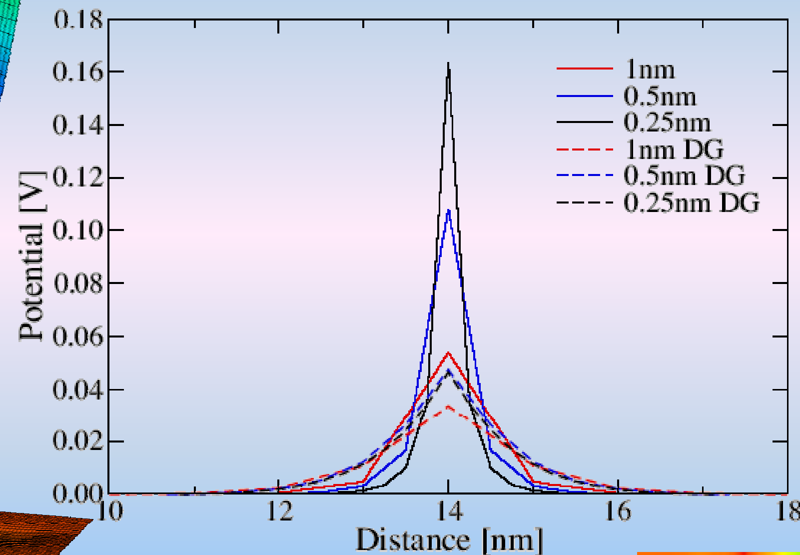
# Quantum correction using Density Gradient

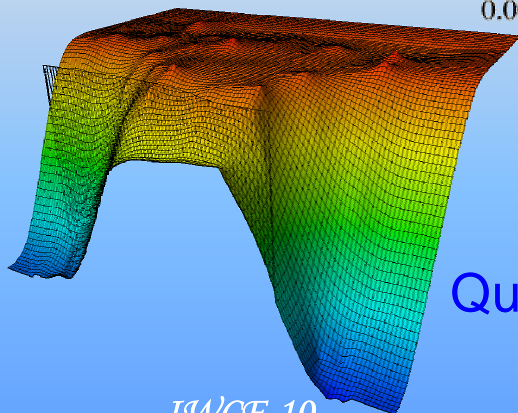


Classical potential

Classical Charge

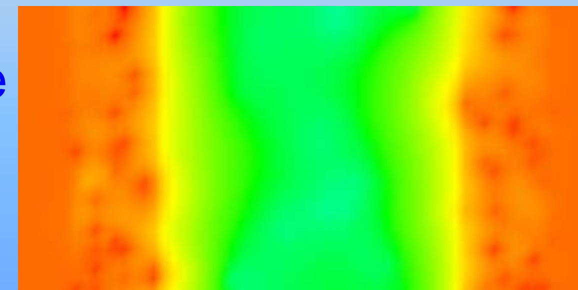


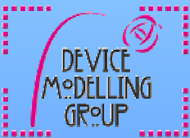


Quantum potential

Quantum Charge





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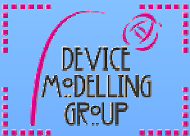

# $V_T$ variation induced by discrete random dopants in scaled devices

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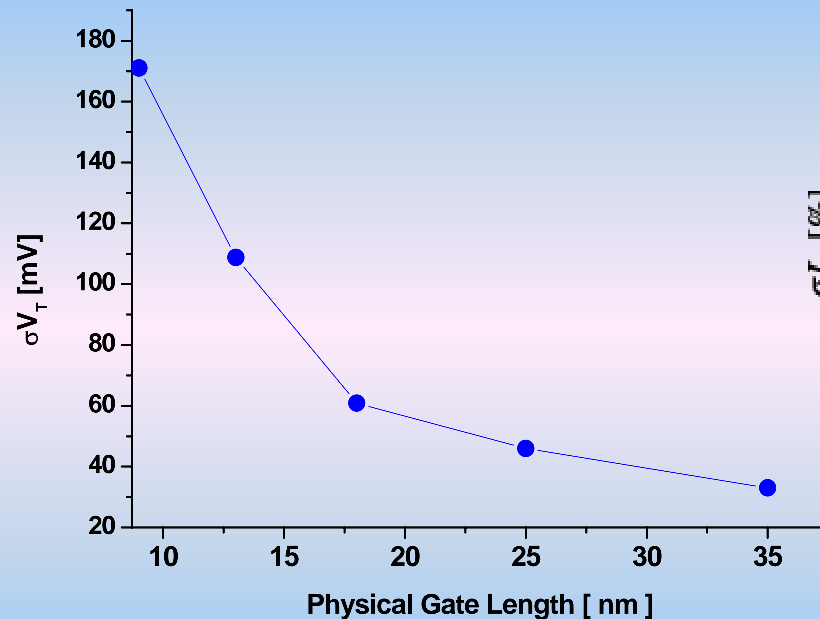
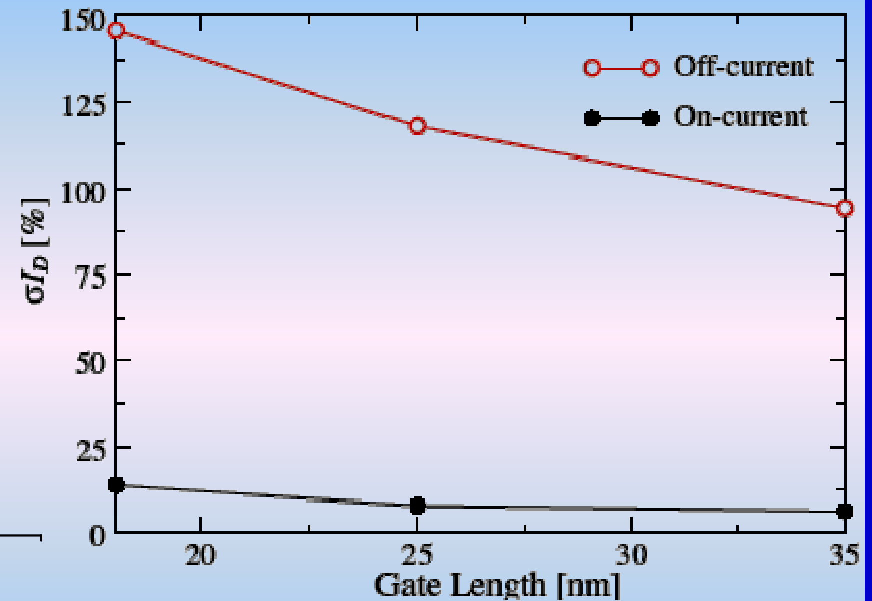
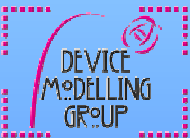



The variation in the threshold voltage increases in every TN

Below 20 nm gate length $\sigma V_T = 60\text{mV}$, and $6\sigma = 360\text{mV}$.

For the 9nm device the $\sigma V_T$=170mV and 6σ = 1020mV.



# $I_{on}$ and $I_{off}$ distribution in the scaled devices

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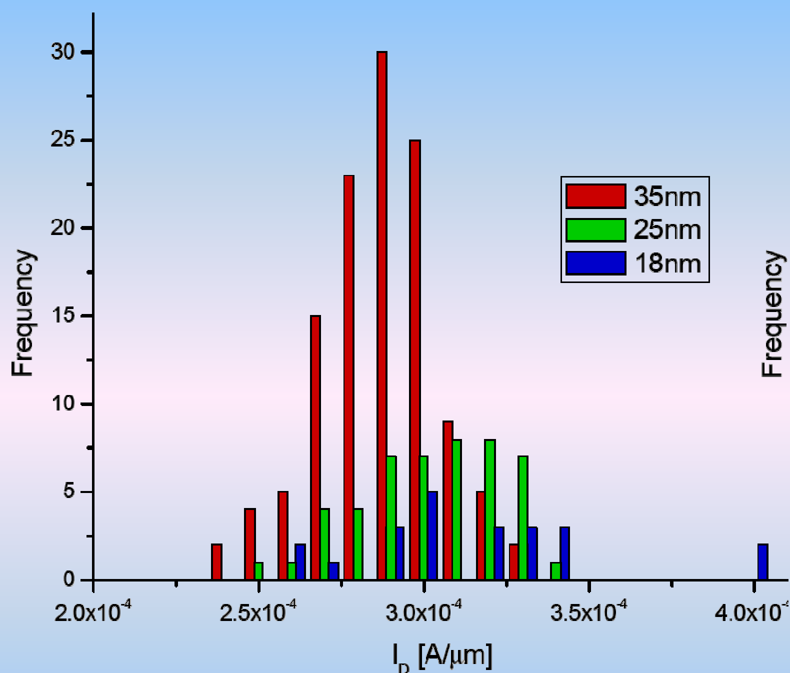
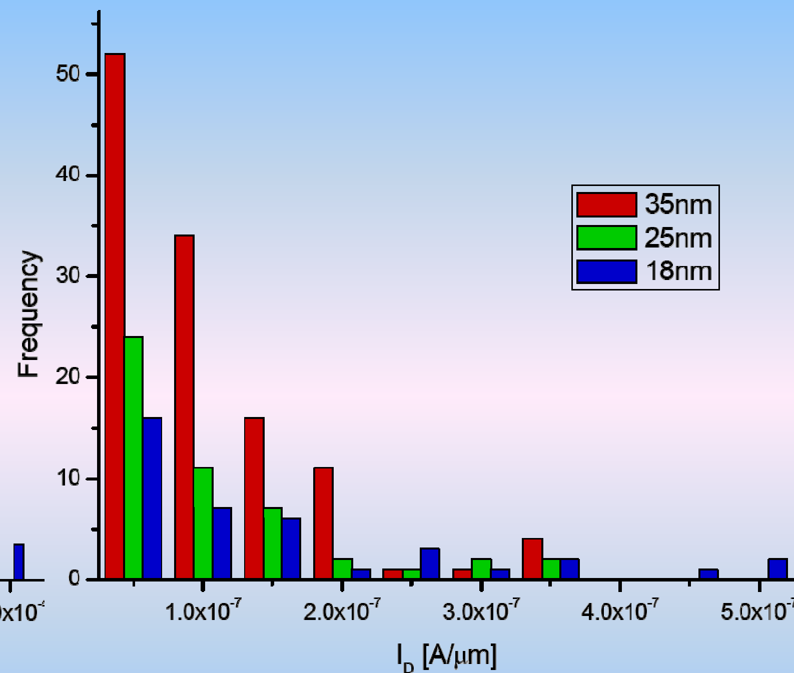
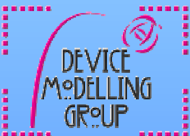



$I_{on}$ distribution of three scaled devices




$I_{off}$ distribution of three scaled devices



# Conclusions

- We have estimated the magnitude of intrinsic parameter fluctuations in realistically scaled devices, which corresponds to all technology node in ITRS 2003 edition.
- $\sigma V_T$ increases in every technology node and reaches more than 150 mV at the end of technology roadmap
- The sub-threshold drain current distribution of the scaled devices highly skewed away from the normal distribution and the $log$ of the off-current should be used for statistical analysis