Three-dimensional quantum transport simulation of ultra-small FinFETs

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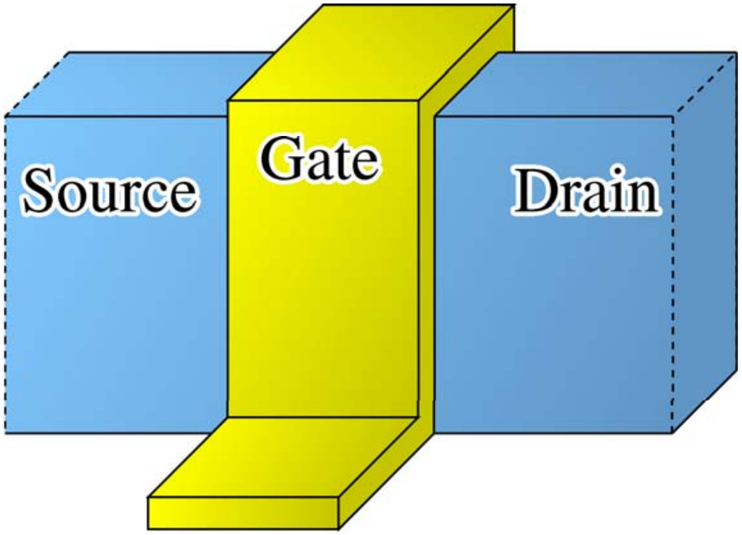
Introduction

- **FinFET :** Non-planar multiple gate MOSFET
- **Quantum Mechanical Effects**
  - Direct S/D tunneling
  - Subband quantization
- **Scattering**
  - Phonon scattering
  - Interface roughness



3D quantum transport simulation

based on NEGF method

3D NEGF Simulation

- Green's function : $G = [EI - H_{xyz} - \Sigma]^{-1}$
- Eigen-mode expansion method

H_{xyz} : Device Hamiltonian

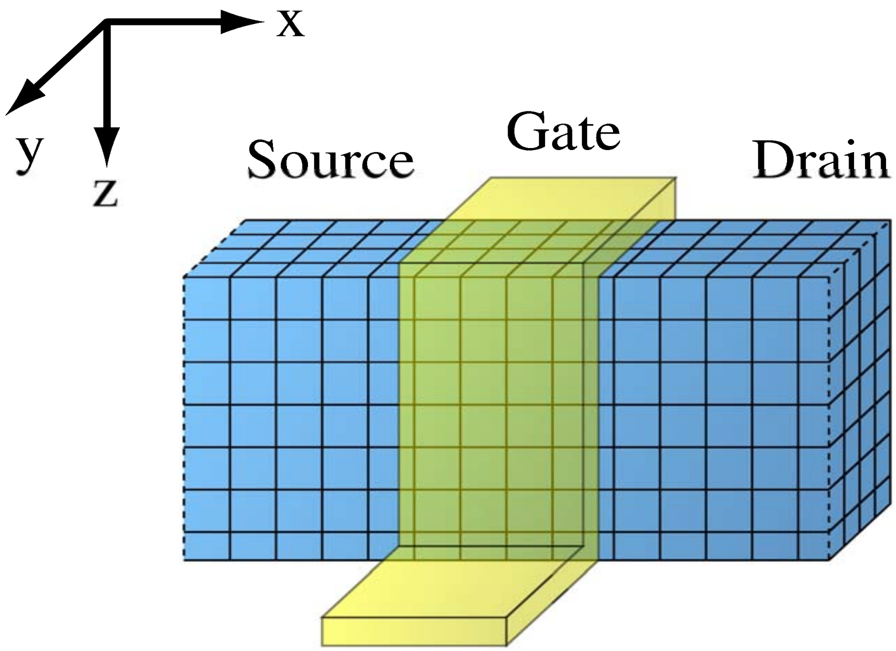
Σ : Self energy

⇒ **3D electron density**

Electric current

- 3D Poisson equation

Self-consistent calculation



Scattering

Intra-valley phonon scattering

- Constant matrix element : $|M(\boldsymbol{q})|^2 = \dfrac{\hbar D_0^2}{2\rho\omega_0}$

$$\hbar\omega_0 = 61.2\,\mathrm{meV}, \quad D_0 = 11.0\times 10^{10}\,\mathrm{eV/m}$$

- Self-consistent calculation :

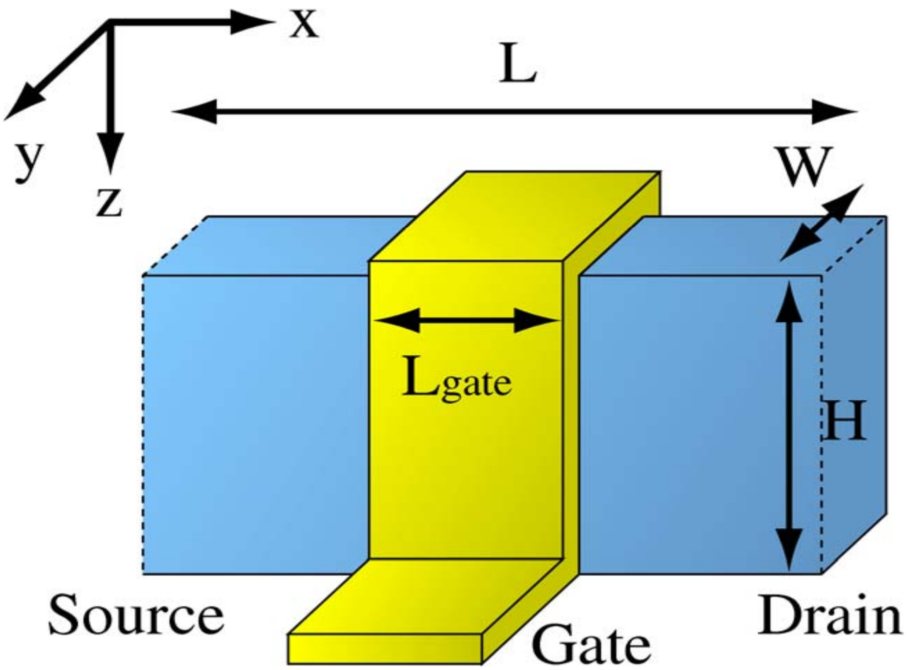
Scattering function (Self energy) ⇔ Green's function (Correlation function)

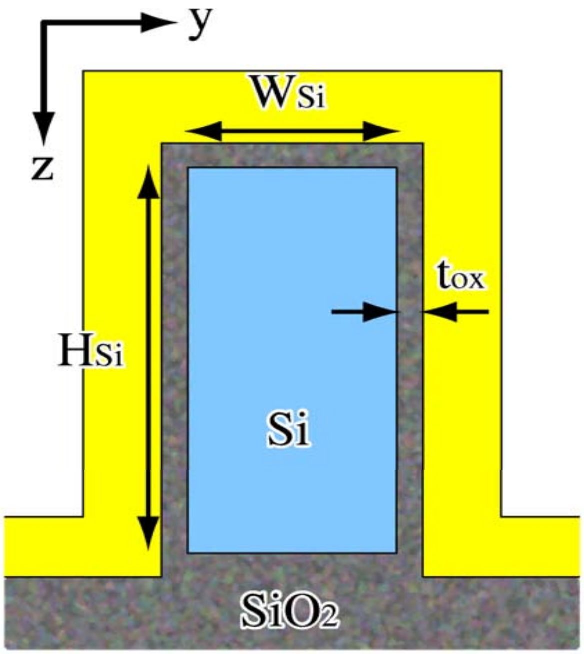
Interface roughness

- Random roughness patterns : $\Delta(\boldsymbol{r}) \longrightarrow V(\boldsymbol{r}), \varepsilon(\boldsymbol{r}), m(\boldsymbol{r})$
- Gaussian form : $\langle\Delta(\boldsymbol{r})\Delta(\boldsymbol{r}')\rangle = \Delta^2 \mathrm{e}^{-(\boldsymbol{r}-\boldsymbol{r}')^2/\Lambda^2}$

Average displacement : Δ, Correlation length : Λ

Device





Gate length : $L_{\text{gate}} = 9\,\text{nm}$

Length : $L = 29\,\text{nm}$

Width : $W = 6\,\text{nm}$

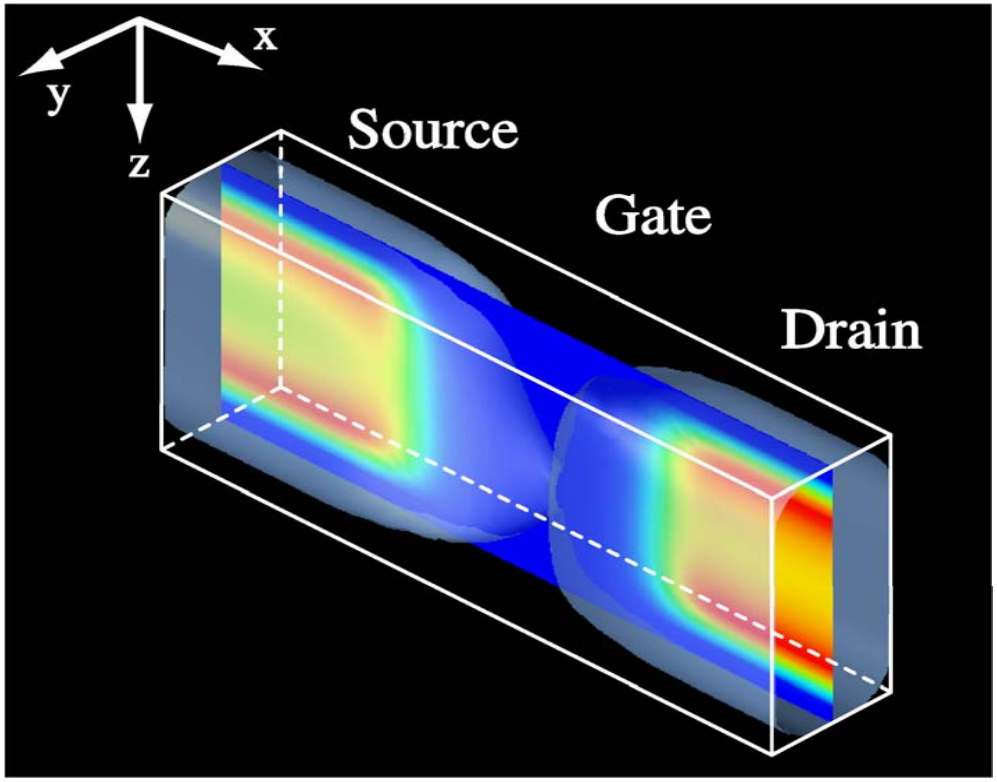
Height : $H = 11\,\text{nm}$

SiO2 thickness : $t_{\text{ox}} = 1\,\text{nm}$

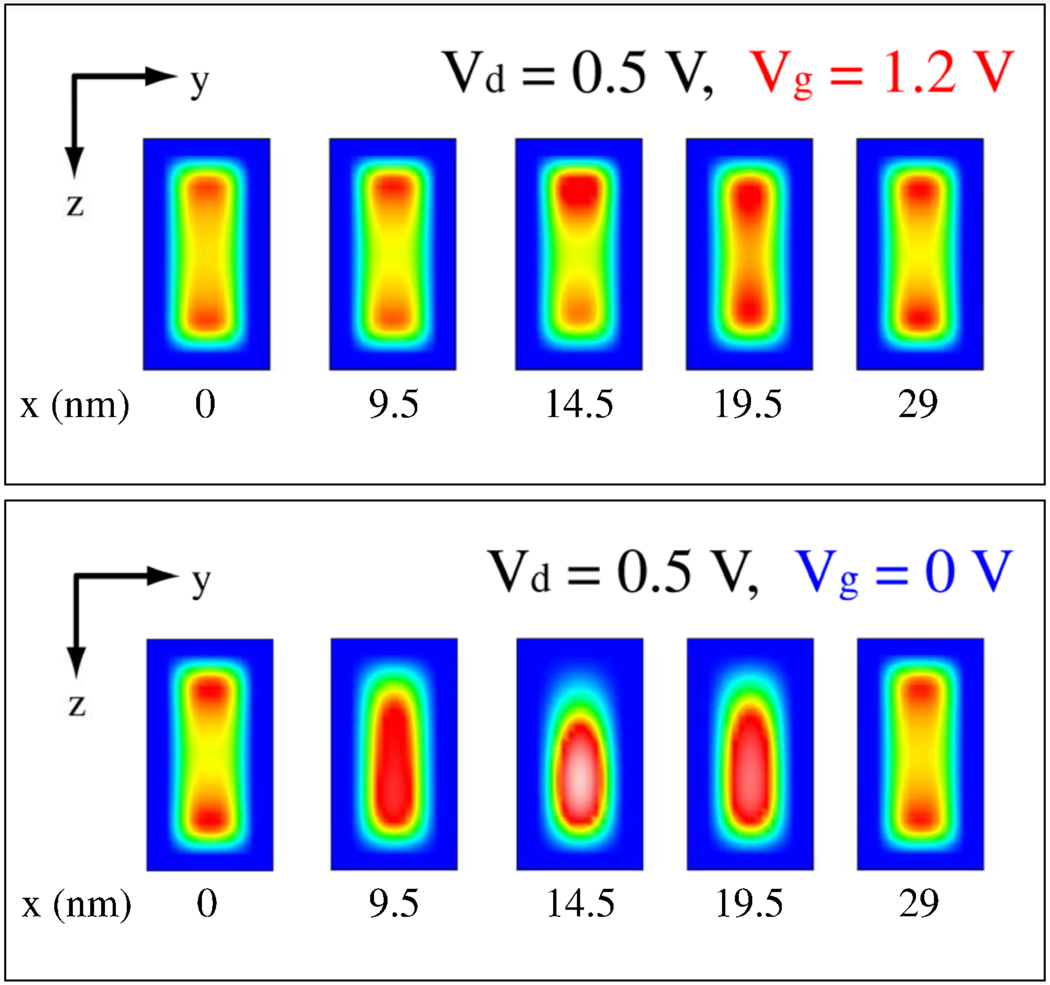
Source / Drain : $N_{\text{D}} = 10^{20}\,\text{cm}^{-3}$

Gate : $N_{\text{A}} = 10^{16}\,\text{cm}^{-3}$

Electron Density

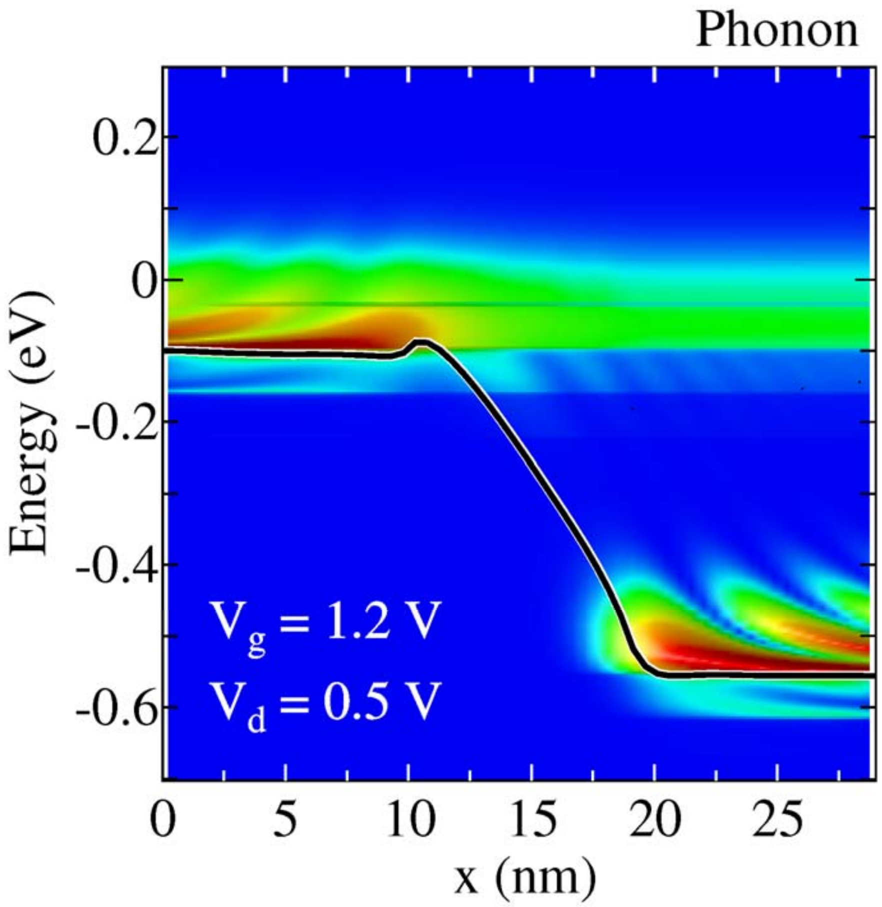


Electron density profile

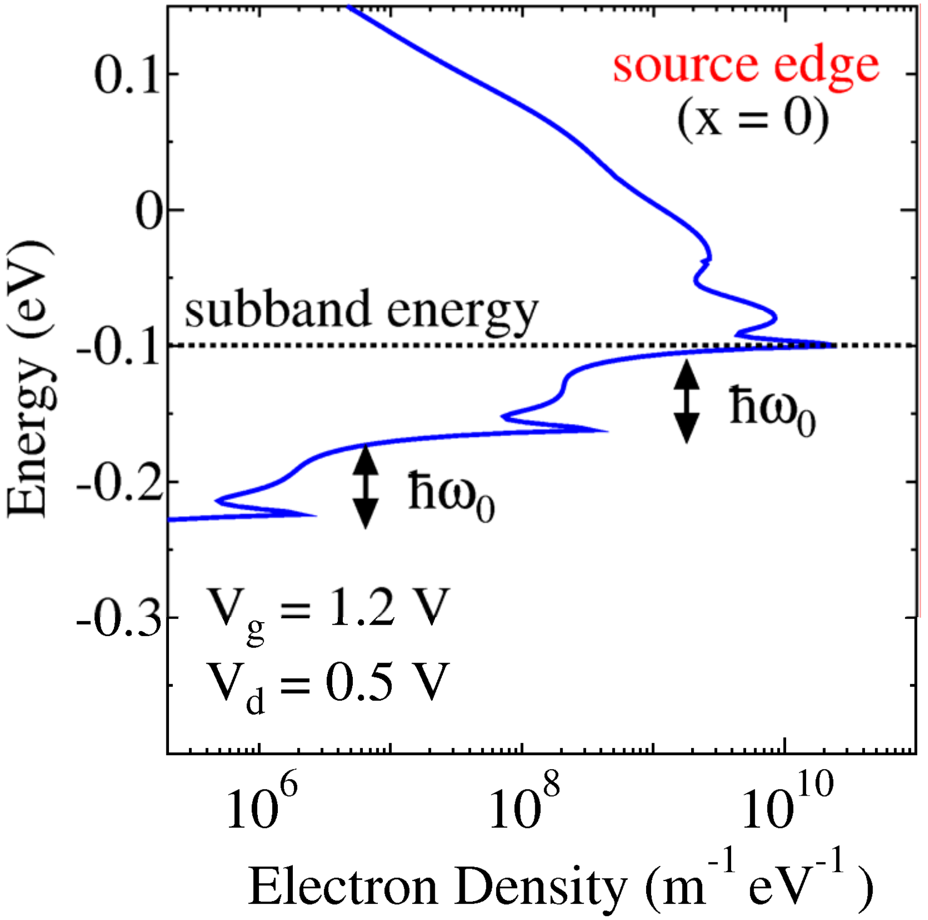


Normalized electron density profile
(*y*–*z* cross section)

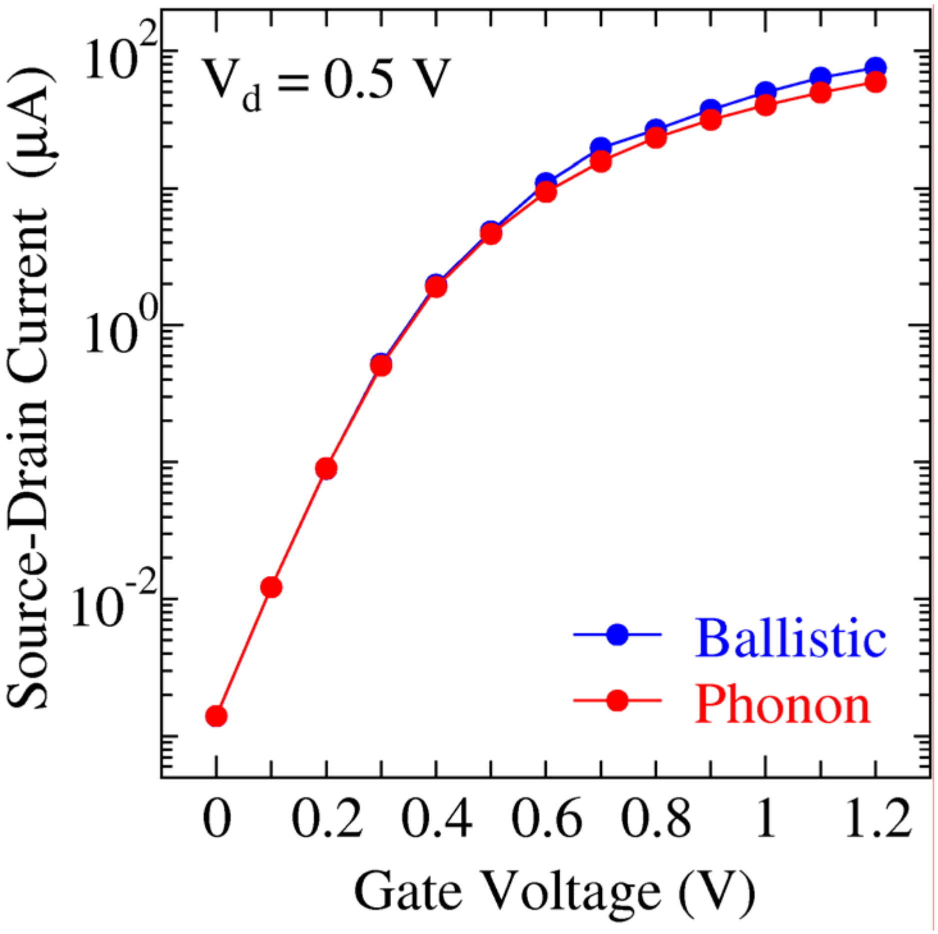
Electron-Phonon Interaction



Electron density profile



Device Characteristics



I_d–V_g characteristics

Ballistic

I_{ON} (V_g = 1.2 V) : 75 μA

I_{OFF} (V_g = 0.0 V) : 1.4 nA

Phonon scattering

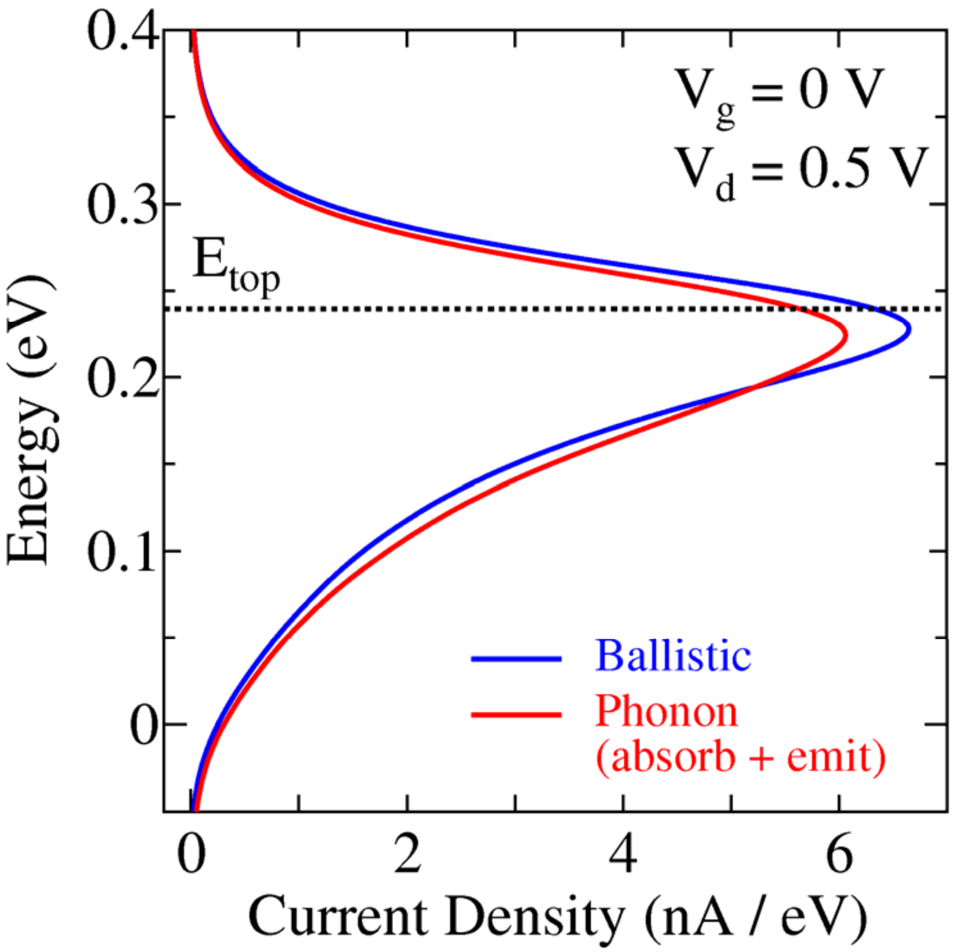
I_{ON} (V_g = 1.2 V) : 60 μA

I_{OFF} (V_g = 0.0 V) : 1.4 nA

About 20% decrease (I_{ON})

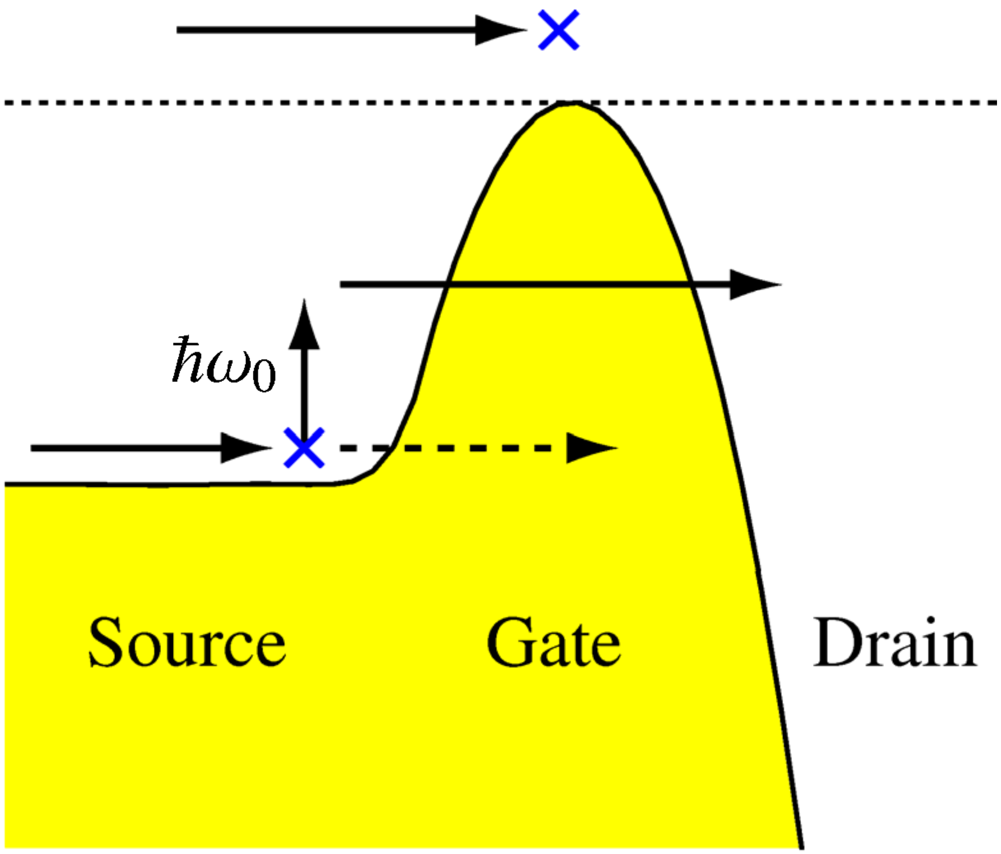
Almost the same (I_{OFF})

Phonon Assisted Tunneling

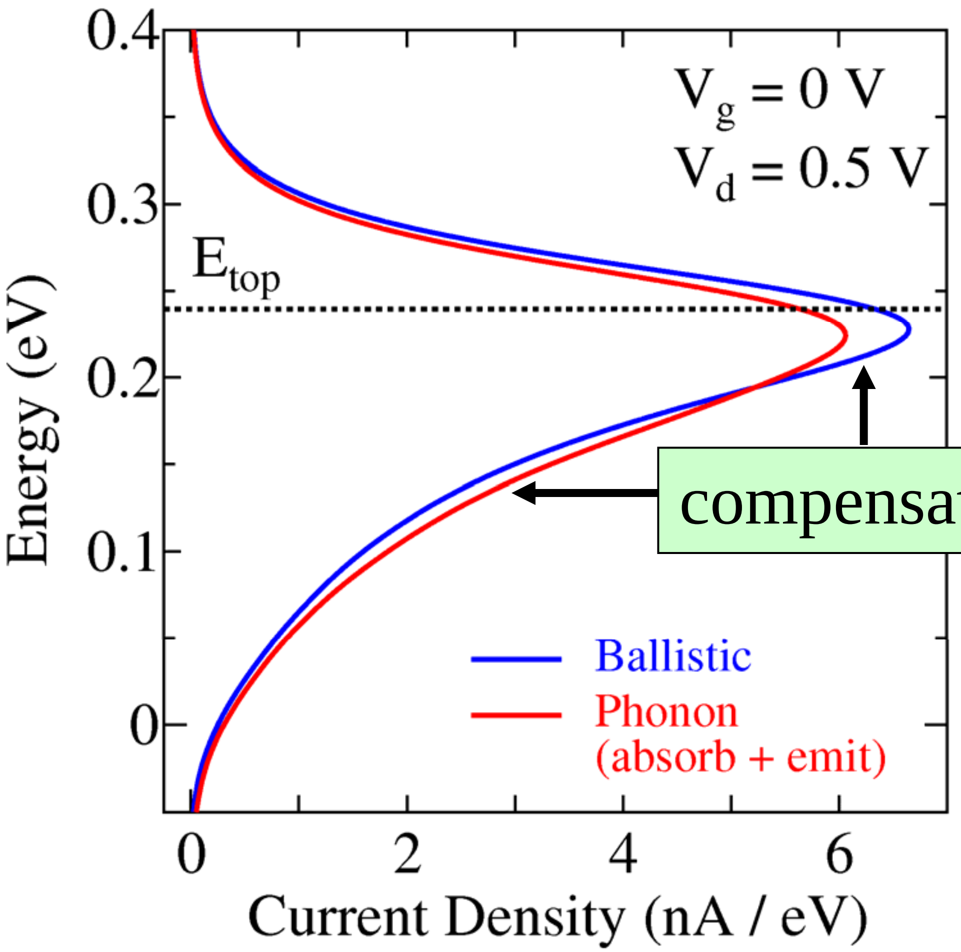


Off-state

Phonon scattering **reduces** current

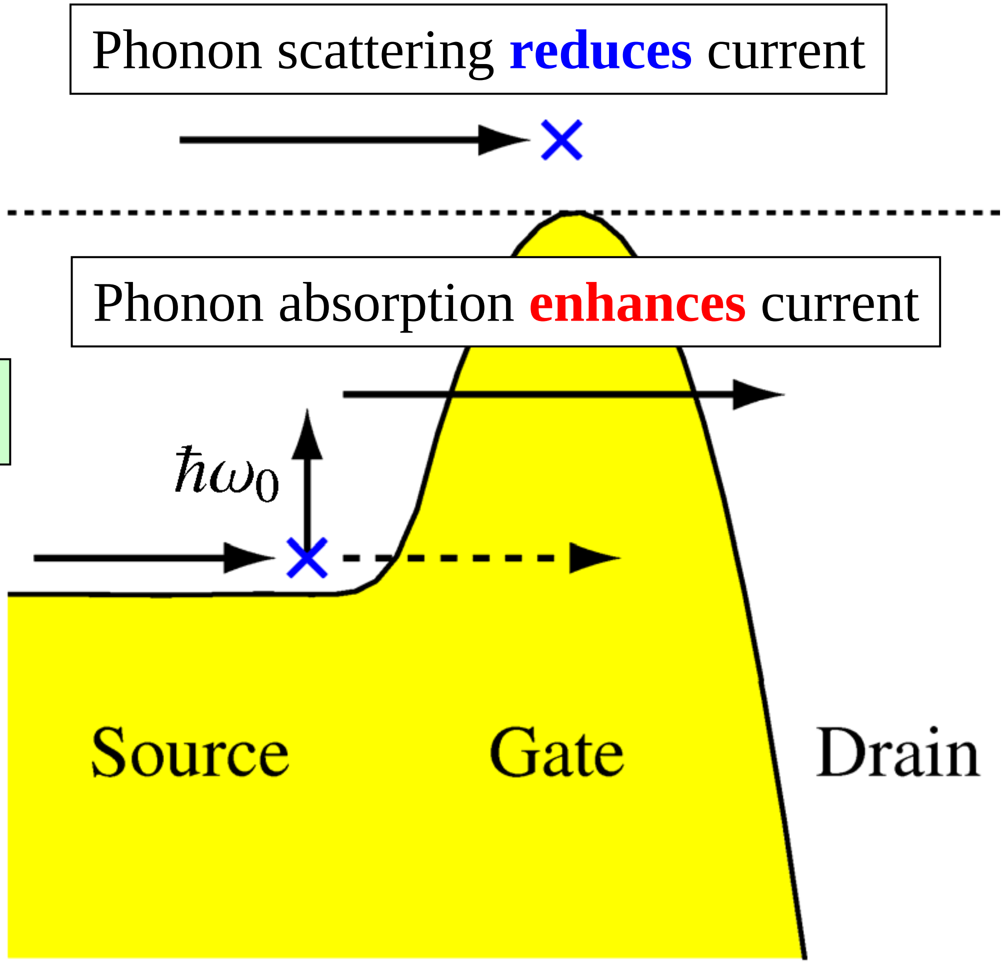


Phonon Assisted Tunneling



compensate

Off-state

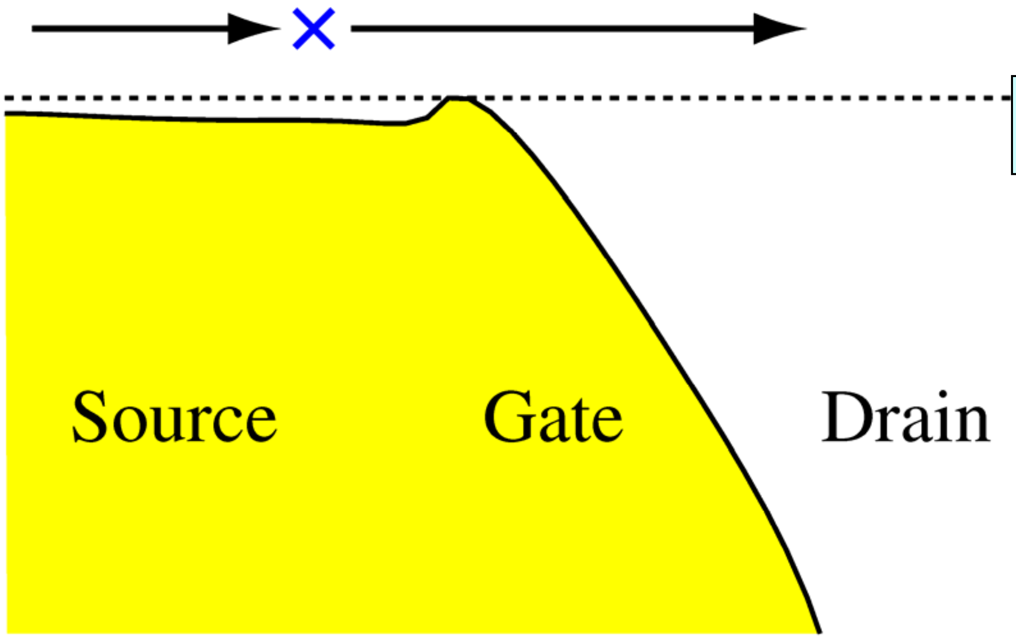

Phonon scattering **reduces** current

Phonon absorption **enhances** current

Phonon Assisted Tunneling

On-state

Phonon scattering **reduces** current

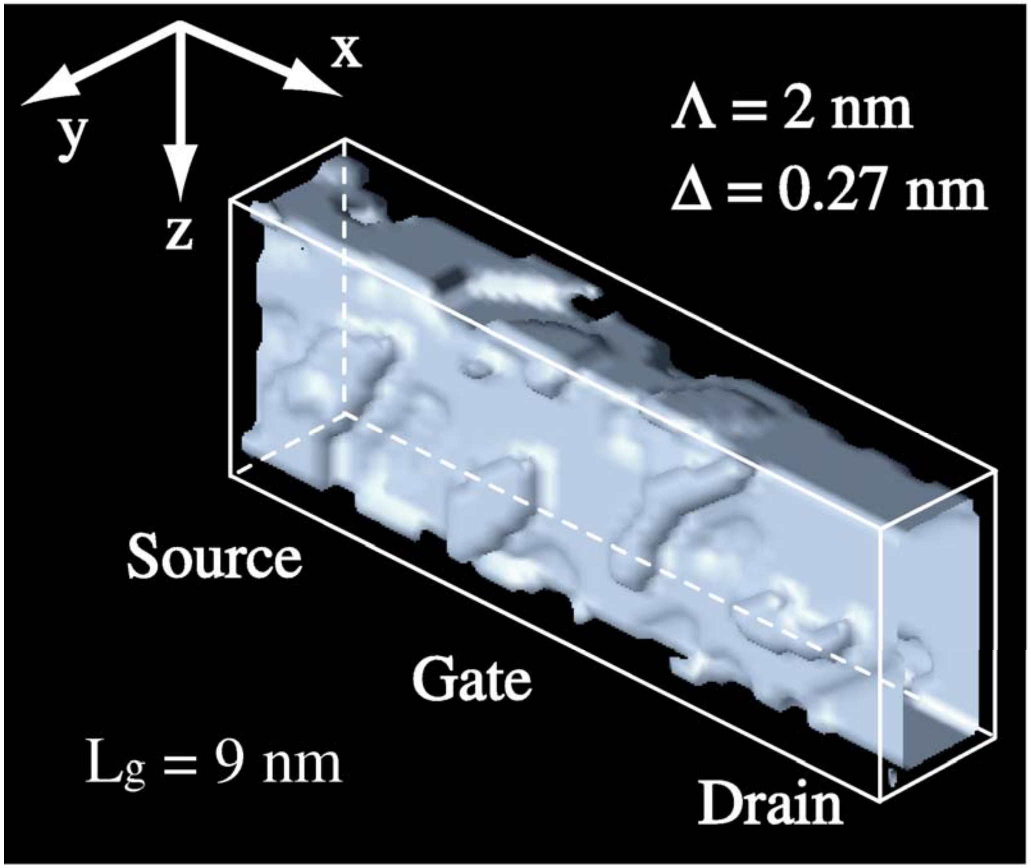


Very low channel barrier

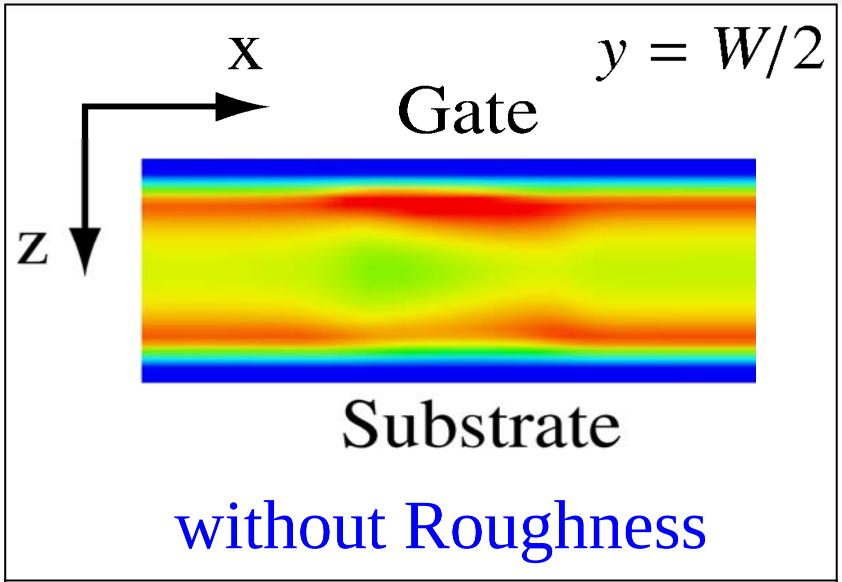
Tunneling current can be **neglected**

Drain current is reduced by phonon scattering

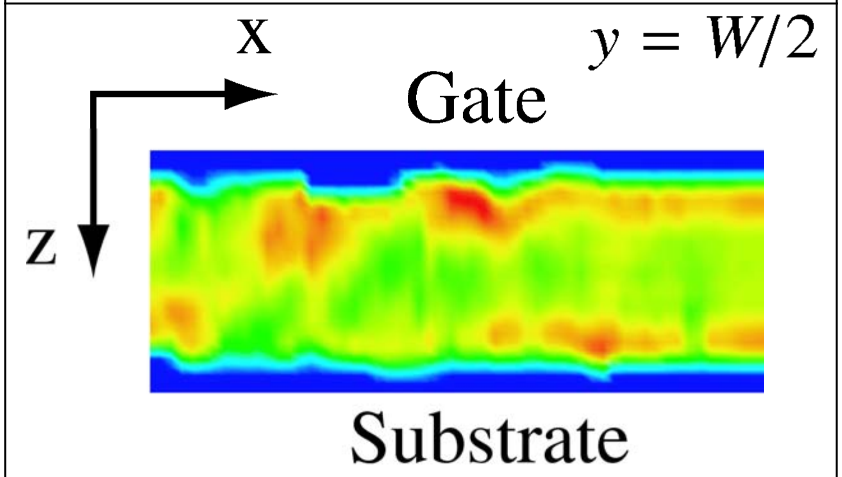
Interface Roughness



Roughness affects current flow

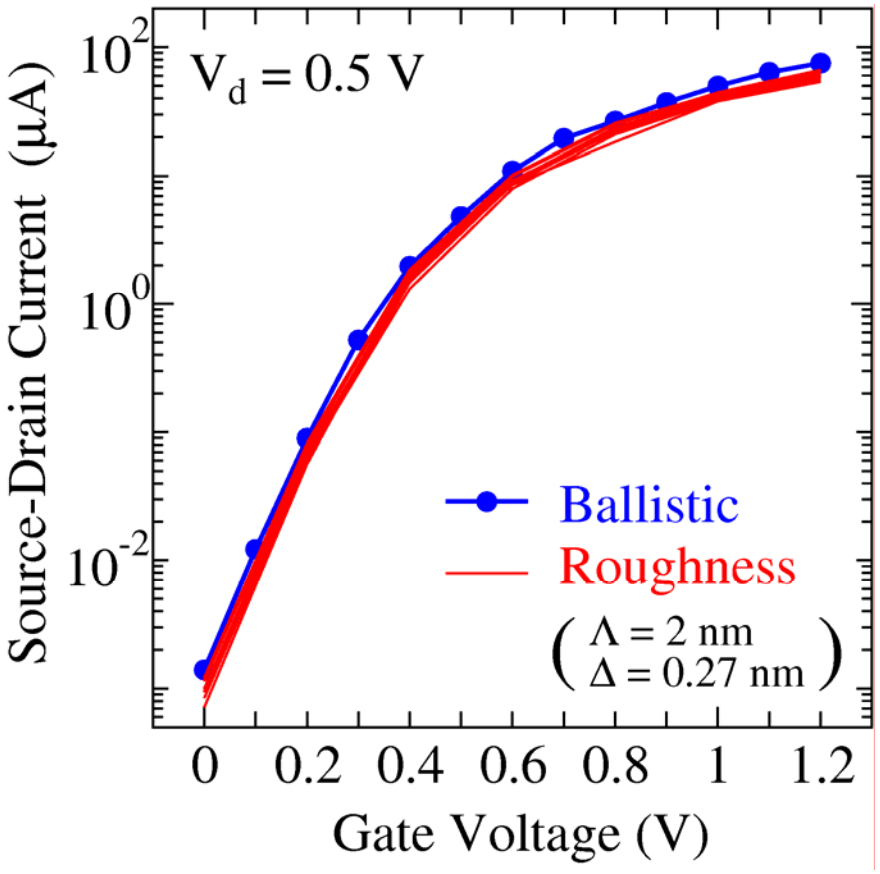


without Roughness



with Roughness

Effect of Interface Roughness



I_d–V_g characteristics

- Roughness : <u>10 patterns</u>
- Threshold voltage (V_{th})

Ballistic

$V_{th} = 0.61$ V

Roughness

$V_{th} = 0.51 \sim 0.62$ V (avg. 0.58 V)

$\sigma(V_{th}) = 35$ mV

Summery

- We have simulated I_d–V_g characteristics of the $9\,\mathrm{nm}$ gate-length FinFETs by 3D NEGF simulation including the **intra-valley phonon scattering** and the **interface roughness**.

- The phonon scattering reduces **only the on-current**.

- The interface roughness affects **not only the on-current but also the off-current**.

- **Large fluctuation of the threshold voltage** is caused by the interface roughness in the ultra-small FinFETs.