OHIO UNIVERSITY

Search for Optimum and Scalable COSMOS

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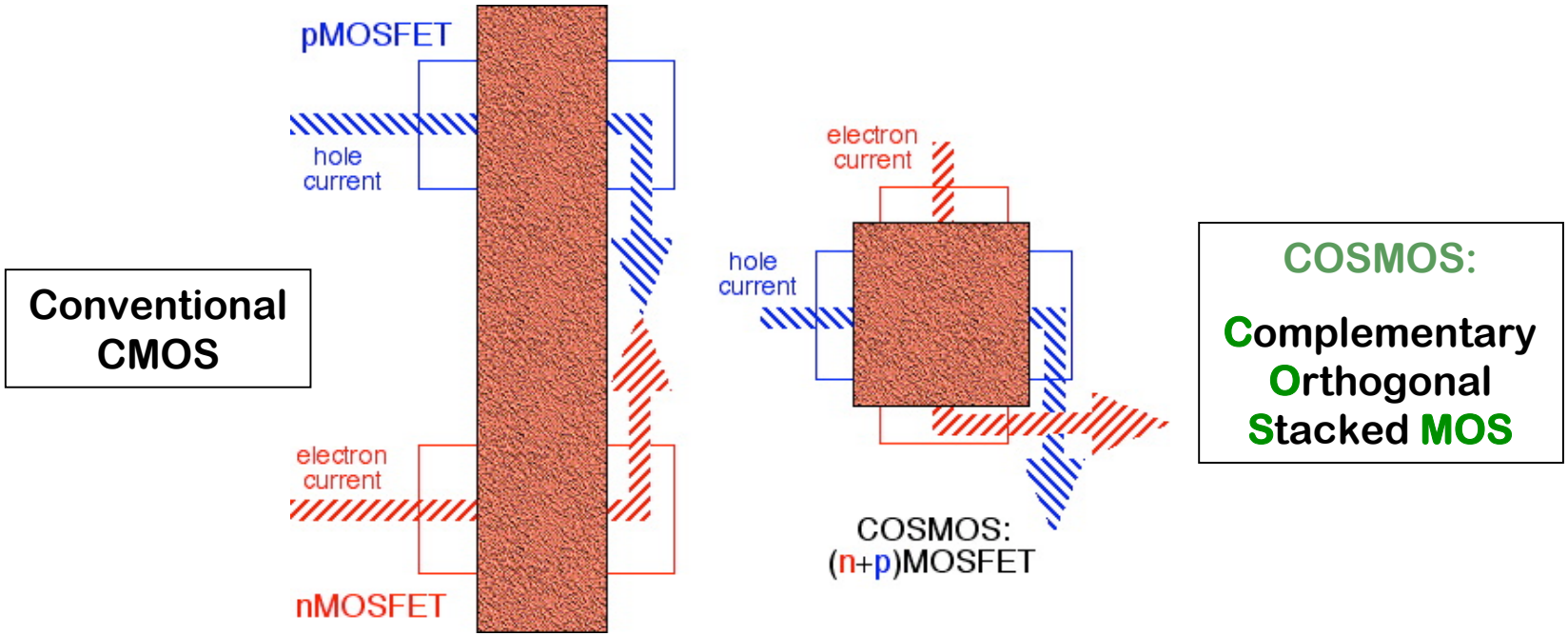
Outline

- Motivation
  - Limitations of Conventional Static CMOS
  - Technology Base
- COSMOS Architecture
- COSMOS Device Operation
- Scaling & Optimization
- Conclusions

Motivation

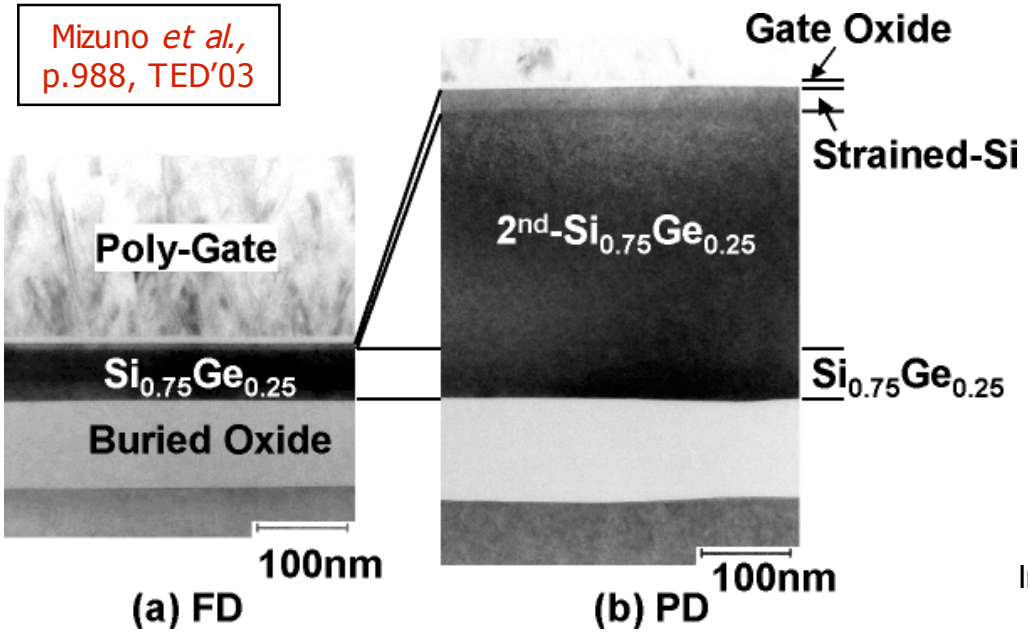
- Vertical + Orthogonal CMOS integration : COSMOS
  - Stack two MOSFETs under a common gate
    - Eliminate the area required for pMOS
  - Improve only hole mobility by using strained SiGe channel
    - pMOS transconductance equal to nMOS
  - Reduce parasitics due to wiring and isolating the sub-nets



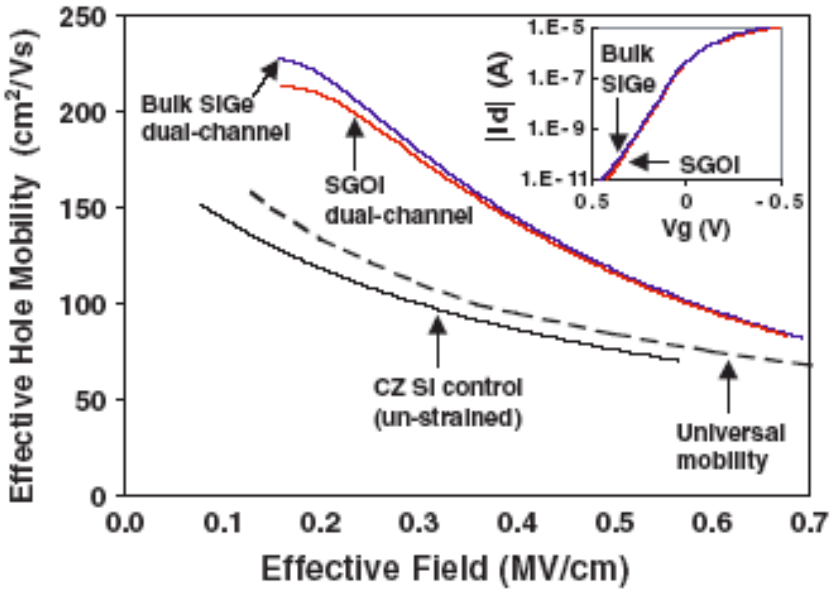
Technology Base

- Strained Si/SiGe layers
  - Built-in strain traps more carriers and increases mobility
    - Equal+high electron and hole mobilities (Jung *et al.*,p.460,EDL'03)
    - Higher Ge%, more the improvements
- SOI (silicon-on-Insulator) substrates
  - active areas on buried oxide (BOX) layer
  - Reduces unwanted DC leakage and AC parasitics

Mizuno *et al.*, p.988, TED'03



Cheng *et al.*, p.L48, SST'04



Inc

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- Motivation
- COSMOS Architecture
  - Layer structure
- COSMOS Devices
- Scaling & Optimization
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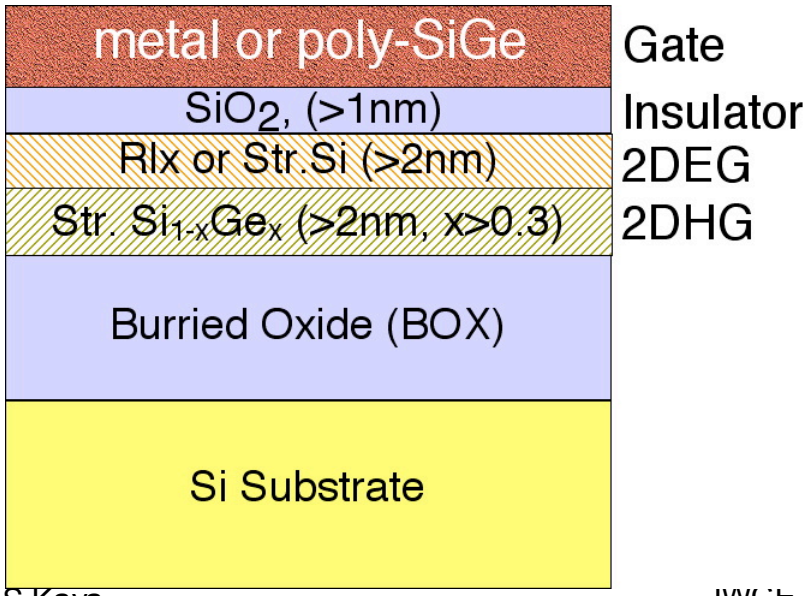
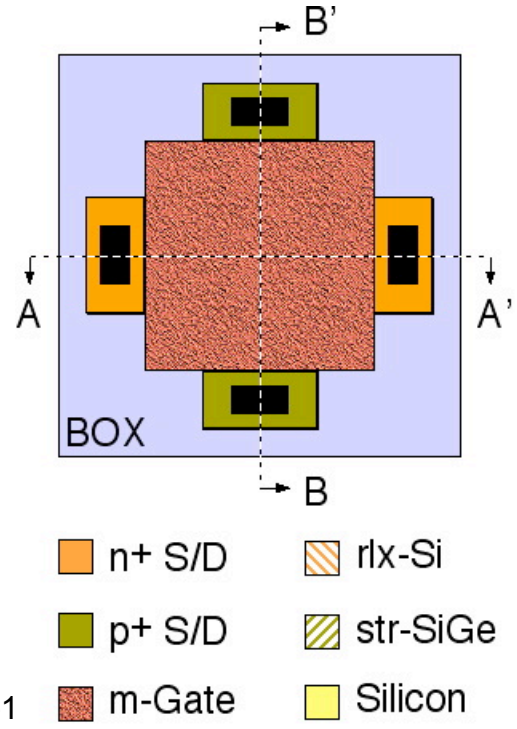
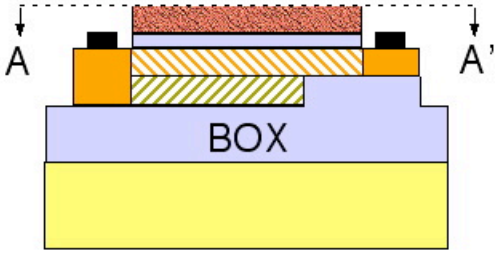
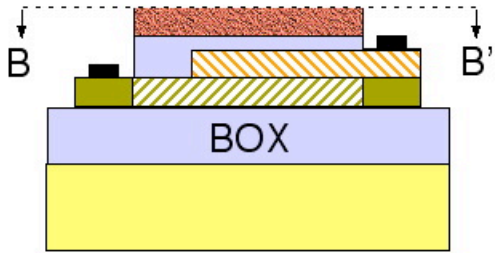
COSMOS Structure

- Single common gate: mid-gap metal or poly-SiGe
  - Must be able to tune for set a symmetric threshold
- Ultra-thin channels: 2-6nm to control threshold/leakage
  - Strained $Si_{1-x}Ge_x$ for holes ($x \geq 0.3$)
  - Strained or relaxed Si for electrons
- Substrate: SOI – mandatory for COSMOS isolation



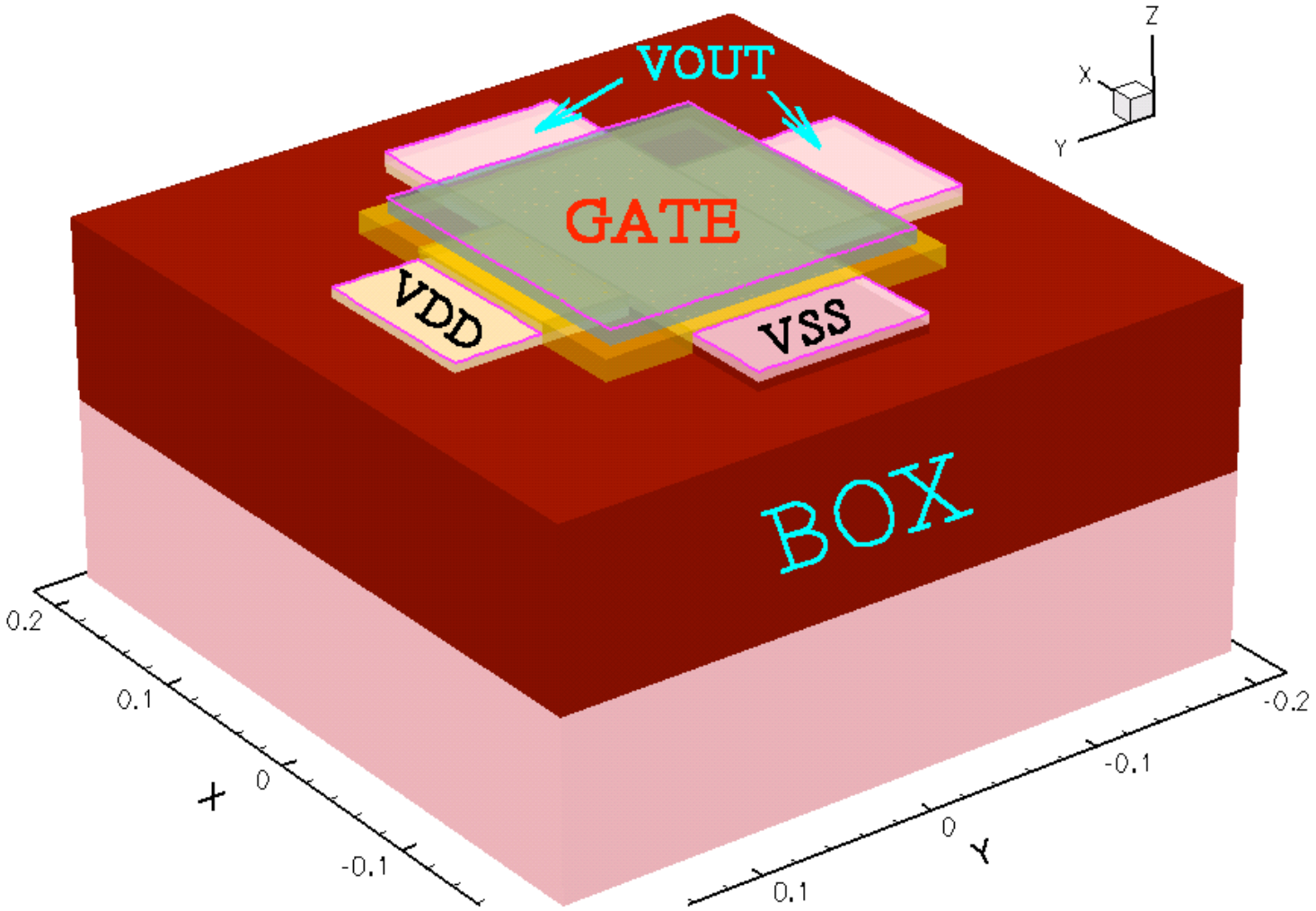






COSMOS Structure - 3D View I

- Single gate stack: mid-gap metal or poly-SiGe
  - Must be engineered for a symmetric threshold

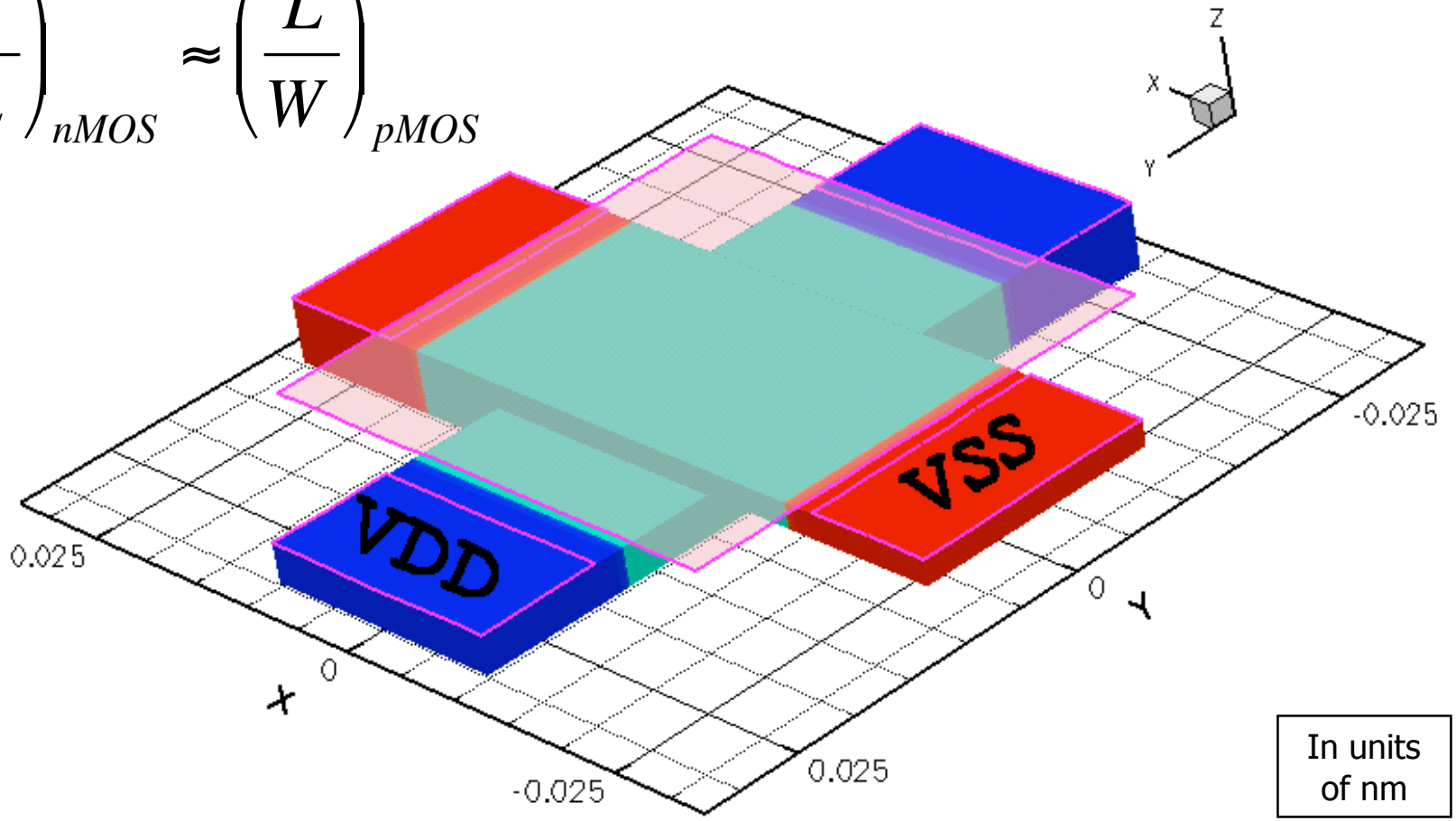


In units of μm

COSMOS Structure - 3D View II

- Conventional self-aligned contacts
  - Doped S/D contacts: p- (blue) or n- (red) type
- Inter-dependence between gate dimensions:

$$\left(\frac{W}{L}\right)_{nMOS} \approx \left(\frac{L}{W}\right)_{pMOS}$$



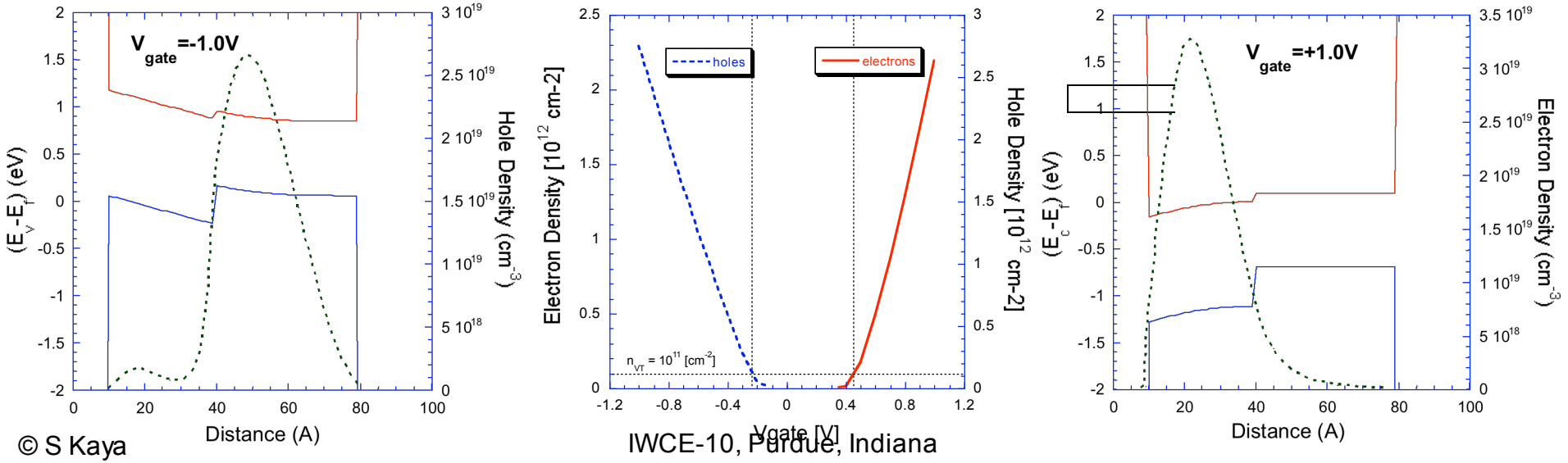
In units of nm

Outline

- Motivation
- COSMOS Architecture
- COSMOS Devices
  - Operation
  - I-V Characteristics
  - Logic Gates
- Scaling & Optimization
- Conclusions

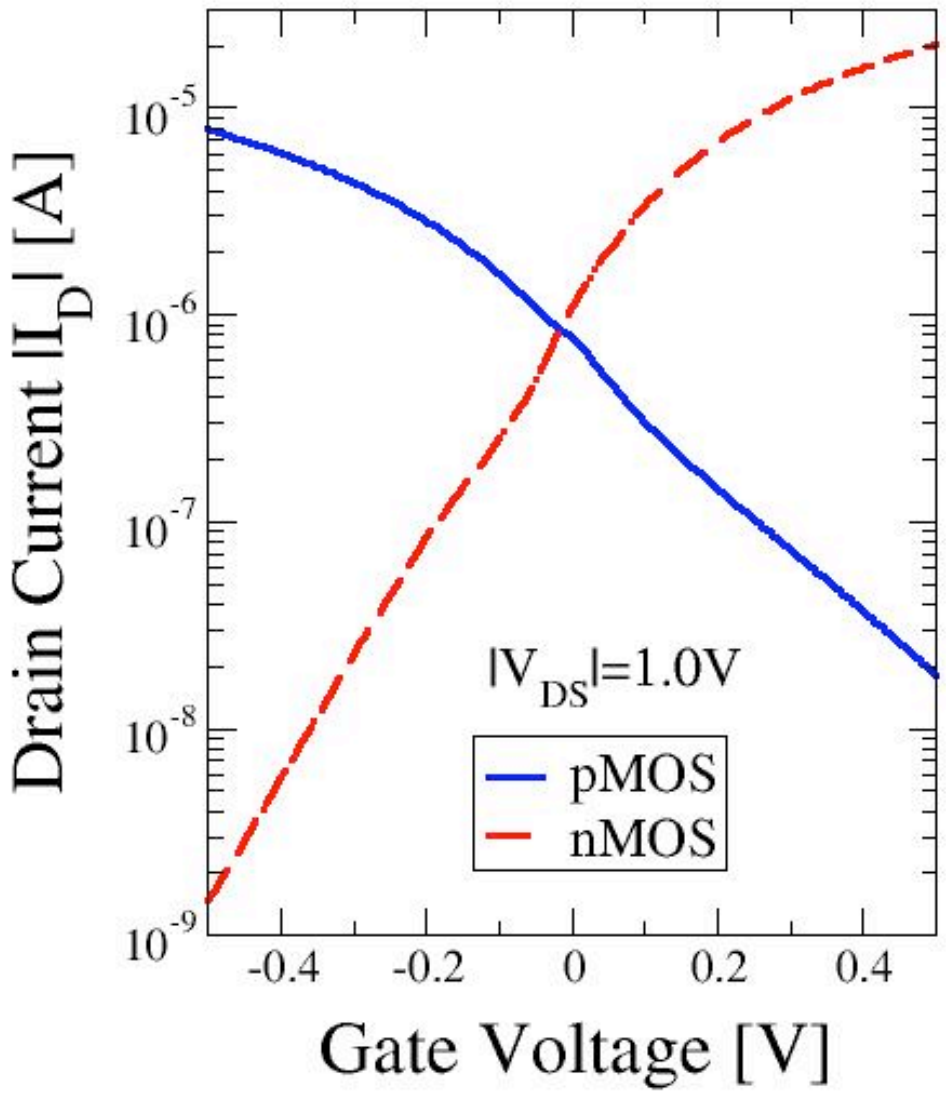
COSMOS Gate Control

- A single gate to control both channels
  - High-mobility strained $Si_{1-x}Ge_x$ ($x \geq 0.3$) buried hole channel
    - High Ge% eliminates parallel conduction and improves mobility
    - Lowers the threshold voltage V_T
  - Electrons are in a surface channel
    - May be relaxed or strained
  - Requires fines tuning for symmetric operation



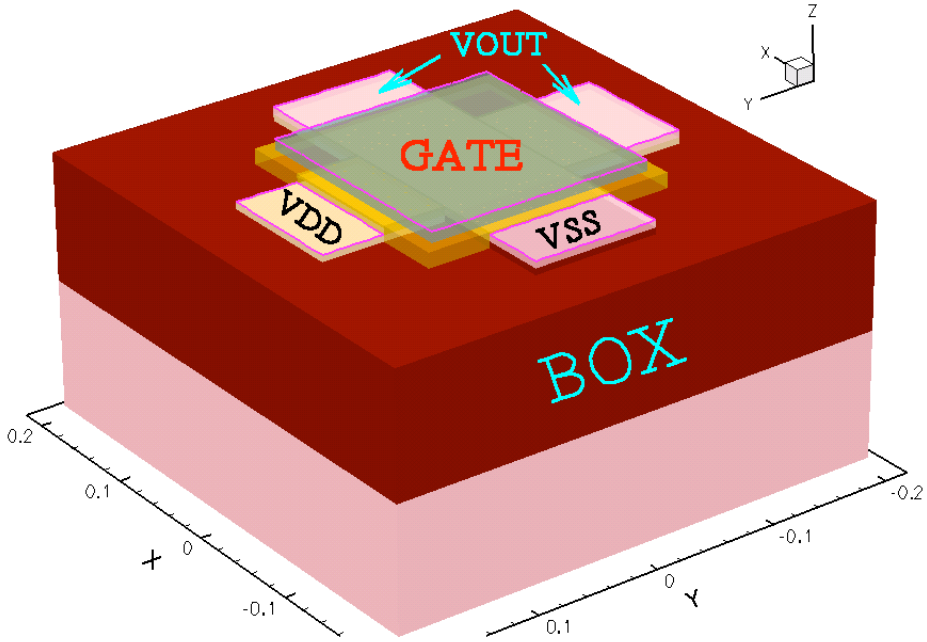
3D Characteristics: 40nm Device

- Symmetric operation
  - No QM corrections
    - Lower VT
  - Features in sub-threshold operation
    - Related to p-i-n parasitic diode included in 3D

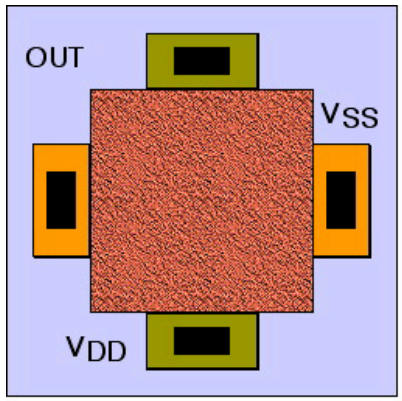


COSMOS Inverter

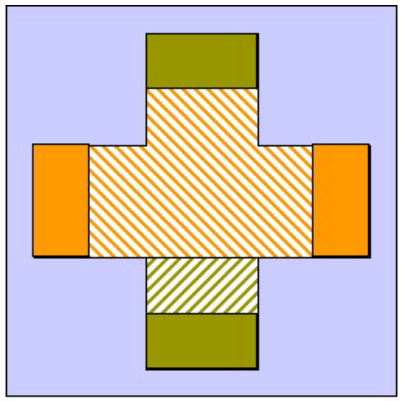
- No additional processing
  - Just isolate COSMOS layers and establish proper contacts
  - Significantly shorter output metallization

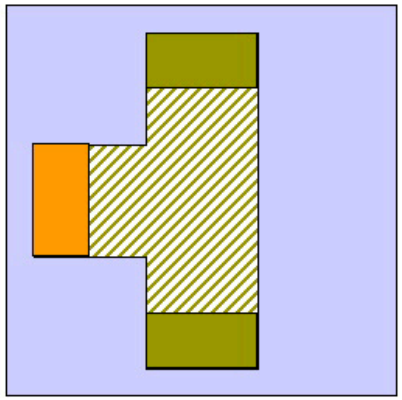


Top view



Peel-off top views



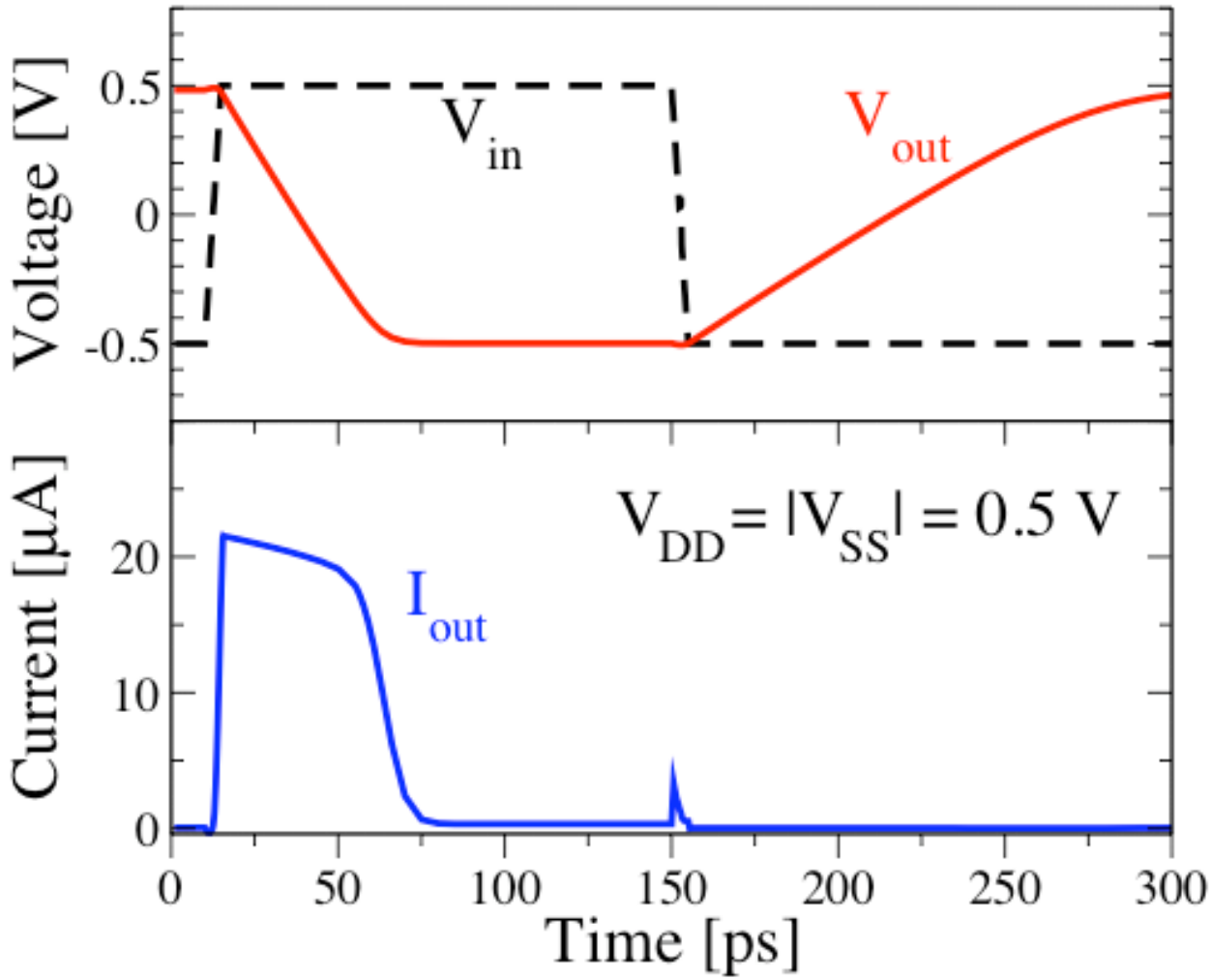


n+ S/D
p+ S/D
m-Gate
rlx-Si
str-SiGe
BOX

COSMOS
NOT Gate

3D TCAD Verification

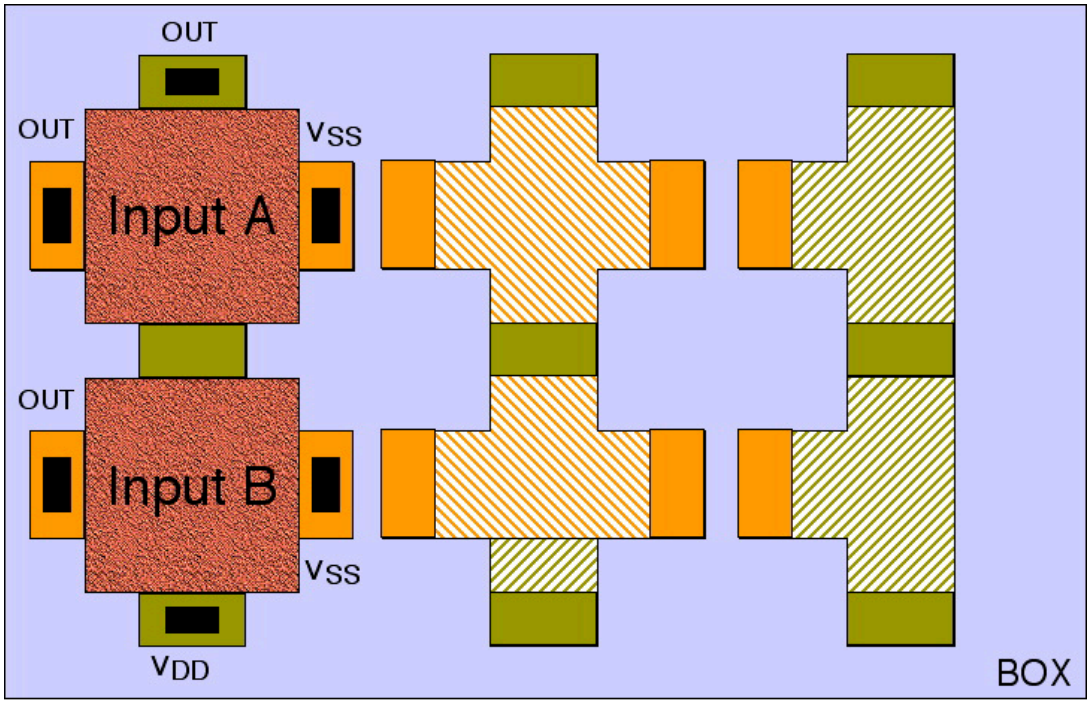
- Inverter operation verified in 3D



40nm COSMOS NOT gate driving C_L=1fF load

Applications

- Low power static CMOS:
  - Should outperform conventional devices in terms of speed
    - Multiple input circuit example: NOR gate
- Area tight designs :
  - FPGA, Sensing/testing, μpower etc. ?



COSMOS NOR Gate

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- Motivation
- COSMOS Architecture
- COSMOS Devices
- Scaling & Optimization
  - Vertical Scaling
  - Lateral Scaling
  - Voltage Scaling
- Conclusions

Vertical Layer Design

- Structural parameters to set V_T for nMOS and pMOS concurrently
  - Design parameters:
    - Ge% in the strained channel: $0.3 \le x \le 0.7$
    - Thickness of the str.SiGe channel: $t_{SiGe} \le 5nm$
    - Gate work-function: $\phi_{n\text{-}polySi} \le \phi_{MS} \le \phi_{p\text{-}polySi}$
    - Si cap thickness: $t_{Si} \le 5nm$
    - SiO_2 equivalent thickness: $t_{ox} \le 2.5nm$
    - Layer order: inverted SiGe/Si layers
- Main design issues:
  - Setting MOS thresholds
    - Symmetric operation
  - Preventing parasitic hole conduction

Nominal parameters:

$\phi_{MS} = \phi_{Si}$ *(midgap)*

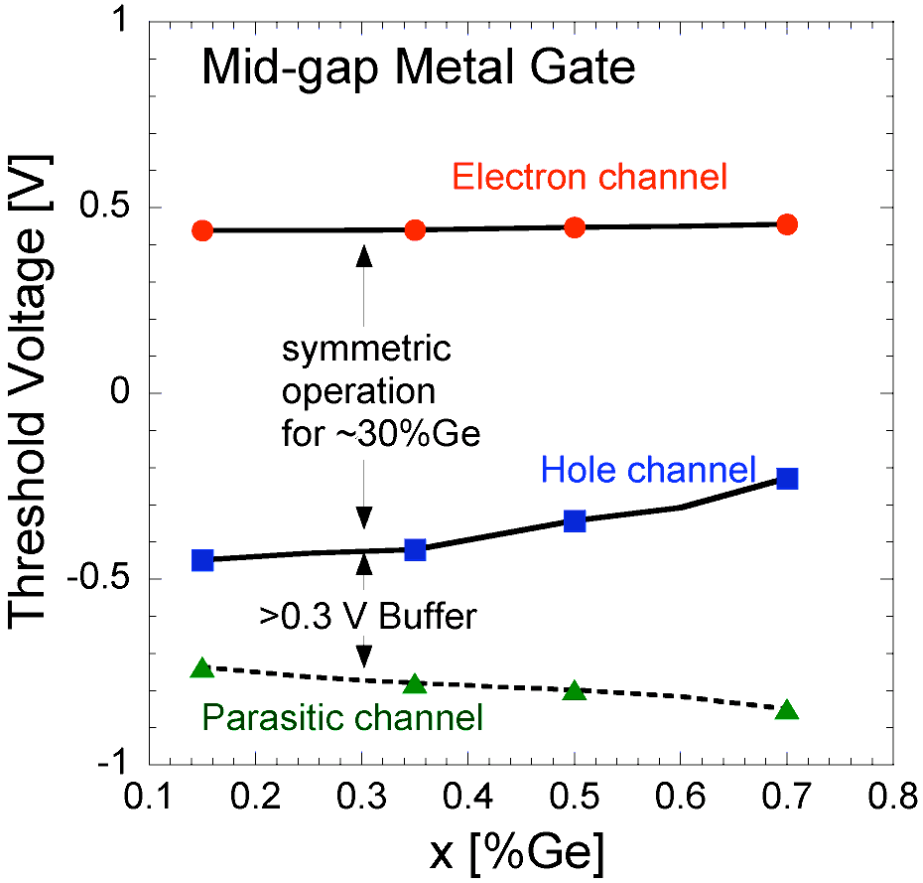
$t_{SiGe} = 3nm$

$t_{Si} = 2nm$

$t_{ox} = 1nm$

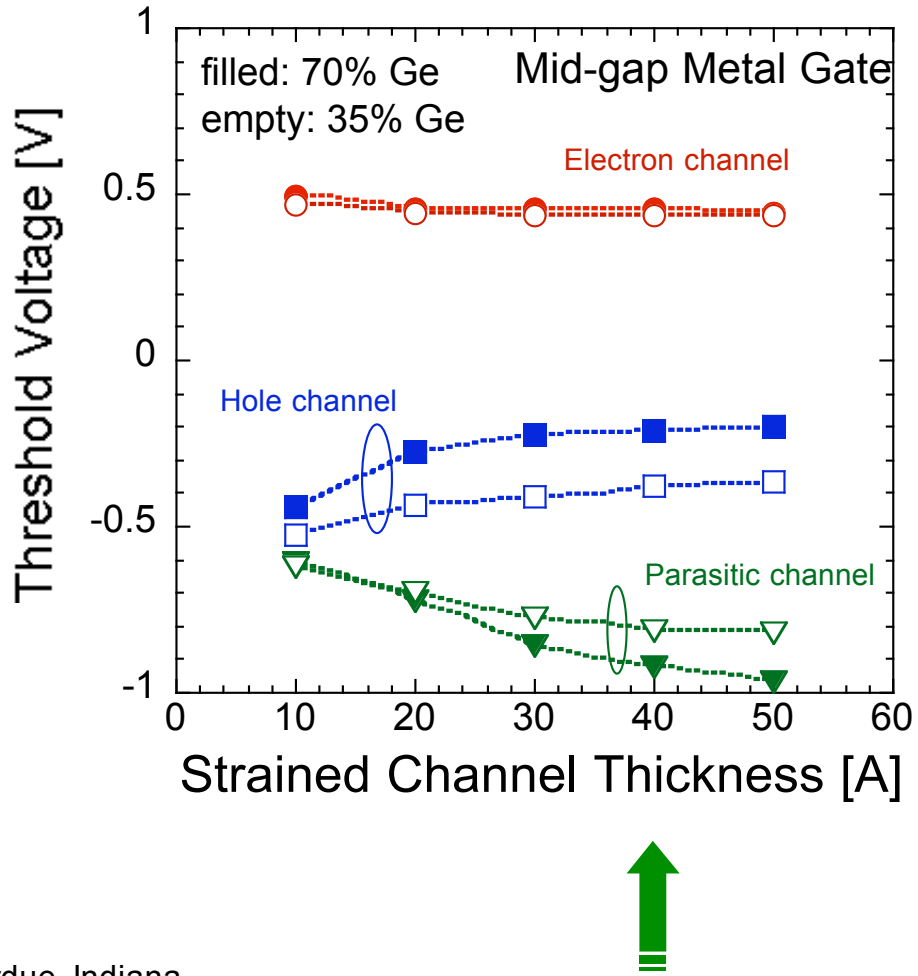
1D Design: Ge%

- Ge% independently sets the pMOS threshold
  - Symmetric operation for a 3nm strained SiGe channel
    - x=0.3 for midgap metal gate
    - x=0.7 requires V_T tuning via channel thickness or gate barrier
  - Parasitic channel
    - Sufficient latitude for design



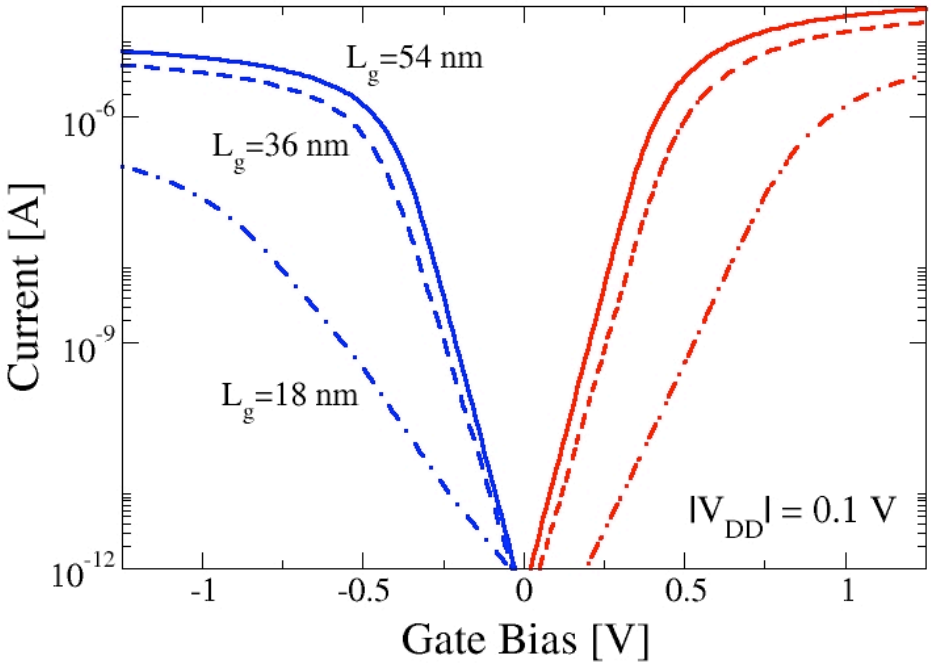
1D Design: Str. SiGe Thickness

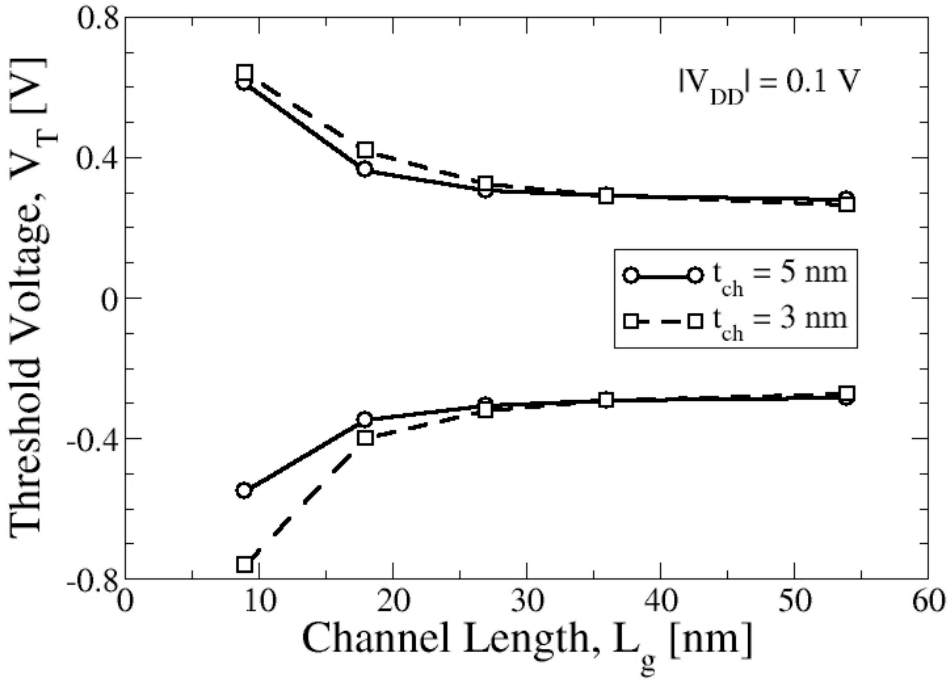
- **Str. SiGe layer thickness mainly influences the pMOS threshold**
  - **Sufficient latitude for design**
  - **Symmetric operation for**
    - **t_{SiGe}=1nm for 70% Ge**
    - **t_{SiGe}=4nm for 35% Ge**
  - **Parasitic channel buffer**
    - **~0.2V for 70% Ge**
    - **~0.45V for 35% Ge**
    - **The thicker SiGe the larger the buffer**



Lateral Scaling

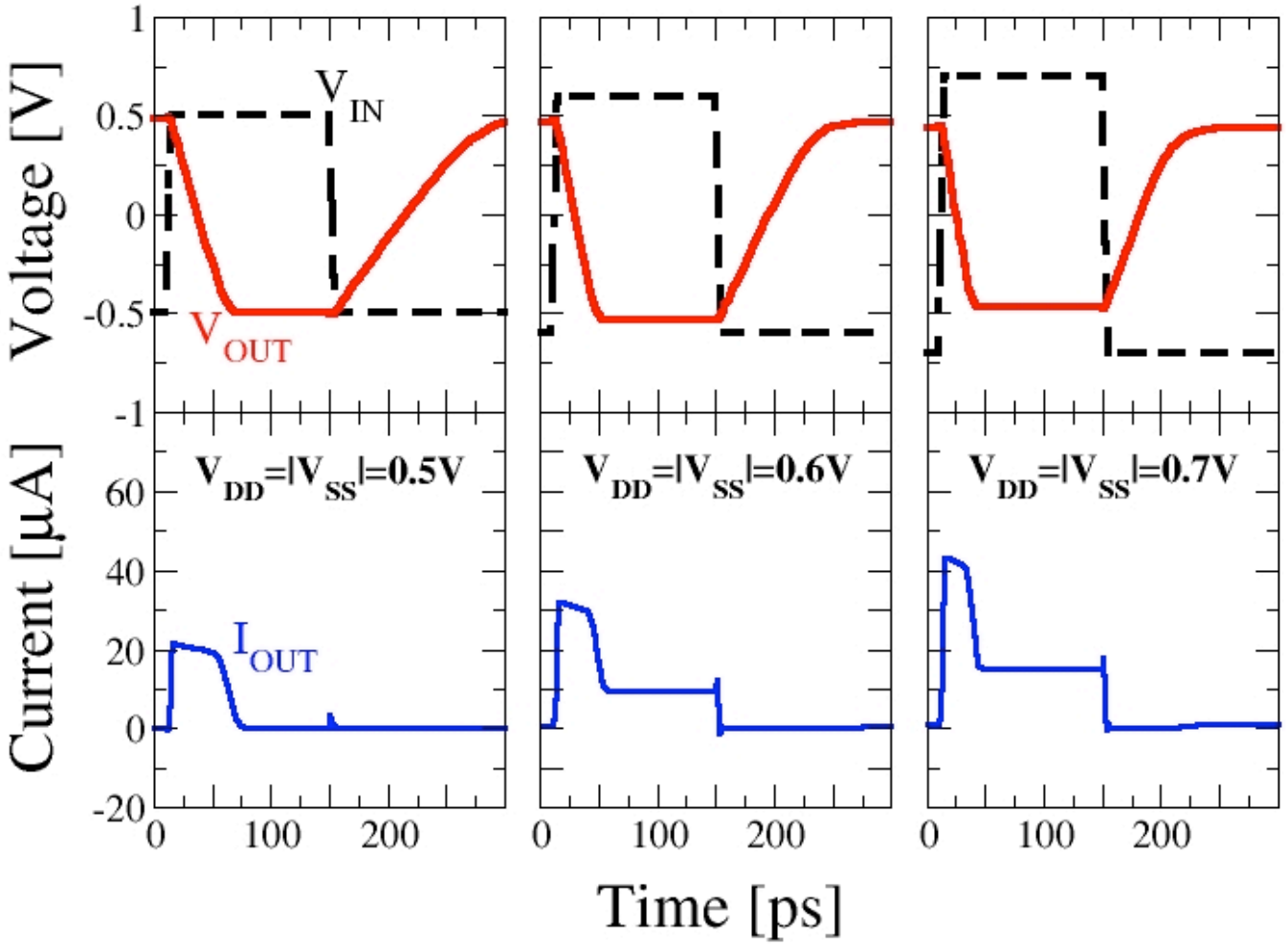
- Unusual (complicated) scaling characteristics
  - for L_g <30nm, I_{DS} reduced and V_T grows
  - Results from reciprocal coupling W/L ratios
- Scaling limit depends on total channel thickness
  - For t_{ch}=5nm, L≥20 nm appears to be reasonable





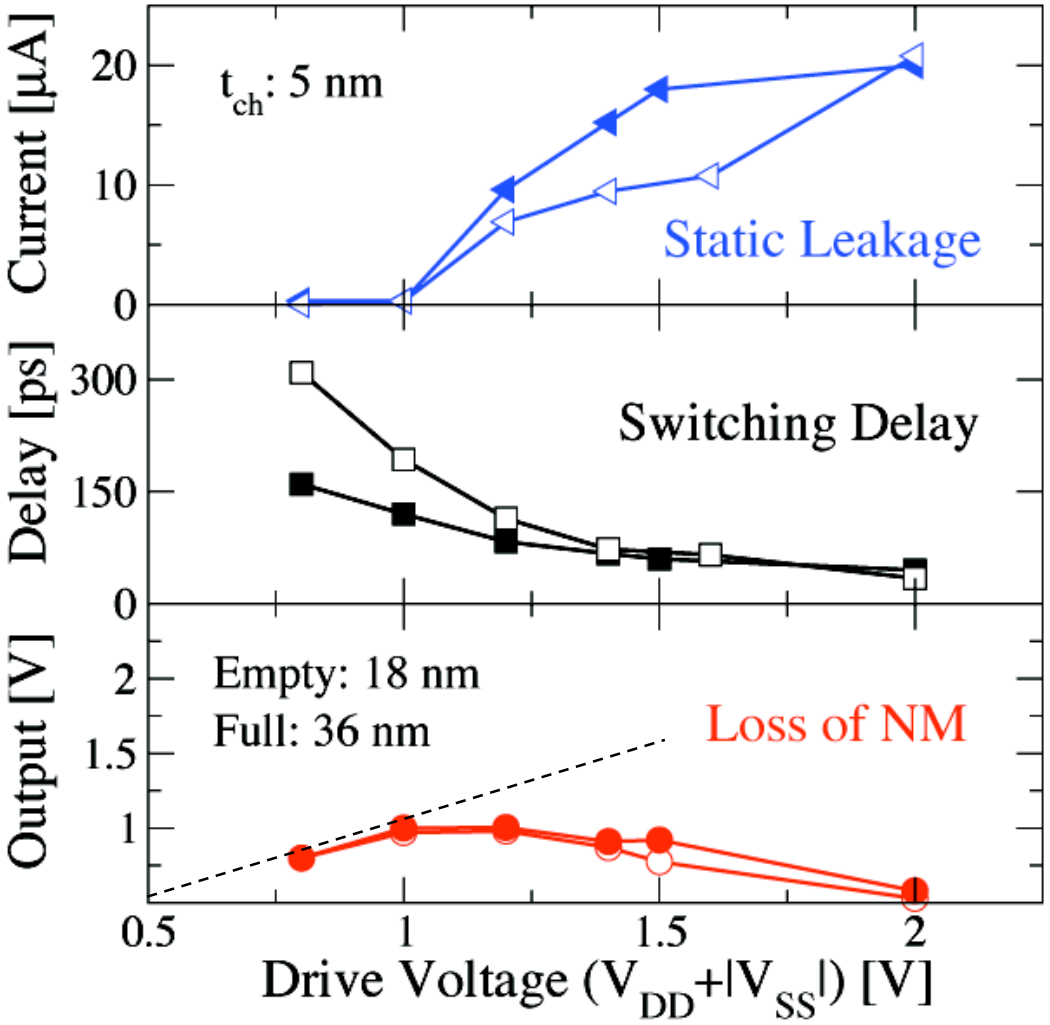
Voltage Scaling (1)

- Significant (~μA) asymmetric static leakage
  - Due to parasitic p-i-n diode turning ON for V_{drive} >1V



Voltage Scaling (2)

- Suitable for low-power applications
  - Limited by static leakage and noise margin
- Figures of merit for 36nm COSMOS @ C_L=1fF , $|V_{DD}|$= 0.5V
  - τ_d ~150ps
  - No loss of NM
  - I_{static} ~ 10 nA



Summary & Conclusions

- Described a novel CMOS architecture
  - COSMOS ⇒ Single gate symmetric CMOS
  - Suitable for low-power & area tight applications
- Used 3D simulations to verify operation
- Identified performance figures and applications
  - ±0.5V bipolar digital operation
  - ~100ns delays => GHz digital operation
  - Limited due to static leakage
- Different scaling behaviour
  - VT grows at smaller gate lengths
  - 20 nm gate length is achievable
  - Concerns for end-of-roadmap (10 nm) requirements.