Analytical and numerical investigation of noise in nanoscale ballistic field effect transistors

G. Iannaccone[1,2]
[1]Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni
Università degli Studi di Pisa, and [2]IEIIT-CNR,
Via Caruso, I-56122 Pisa, Italy

email: g.iannaccone@iet.unipi.it website: http://www.iet.unipi.it/~d8666

Major semiconductor companies have already announced the fabrication of perfectly functional MOSFETs with channel lengths in the range 8-15 nm. Integrated circuits based on millions ofù such devices are expected to reach the marked in the next few years, as predicted by the International Technology Roadmap for Semiconductors. In devices with such short channel lengths, ballistic transport may play a significant role [1]. In addition, the gate oxide is thinner than 1 nm, therefore tunneling through the oxide is not negligible.

In this paper, we focus on shot noise of the drain and gate currents in ballistic MOSFETs. The subject is of interest from the point of view of applications, since adequate models of noise in such MOSFETs are required, especially for high-frequency analog and mixed-signal applications, and from the point of view of the understanding of the underlying physics, since effects typical of mesoscopic devices can now be observed at room temperature and in silicon.

Shot noise in multimode ballistic conductors, a class of devices including MOSFETs, has been recently investigated in Refs. [2] and [3]. Suppression of shot noise has been predicted as a result of Fermi statistics at the source contact, and of electrostatic interaction in the channel. With respect to the mentioned papers, we focus on realistic MOSFET structures, to evaluate quantitatively shot noise power spectral density, and whether the suppression is measurable. To such aim, we use a model already developed for the simulation of the DC characteristics of nanoscale ballistic MOSFETs [4]. We show that, in the range of operating gate-to-source and drain-to-source voltage, shot noise can be suppressed down to less than 10% of the value for a Poissonian process, at room temperature. Such suppression must be taken into account in accurate compact models of device noise to be used in circuit simulation.

Shot noise in the gate current has been previously investigated by the author [5]. New results are presented, showing that noise is suppressed as a result of trap-like defects in the oxide, typically due to aging and/or electric field stress (Fig. 2). Given that the gate current is not always negligible with respect to the drain current, an appropriate model of shot noise is the gate current is of interest also for applications.

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A full journal publication of this work will be published in the Journal of Computational Electronics.

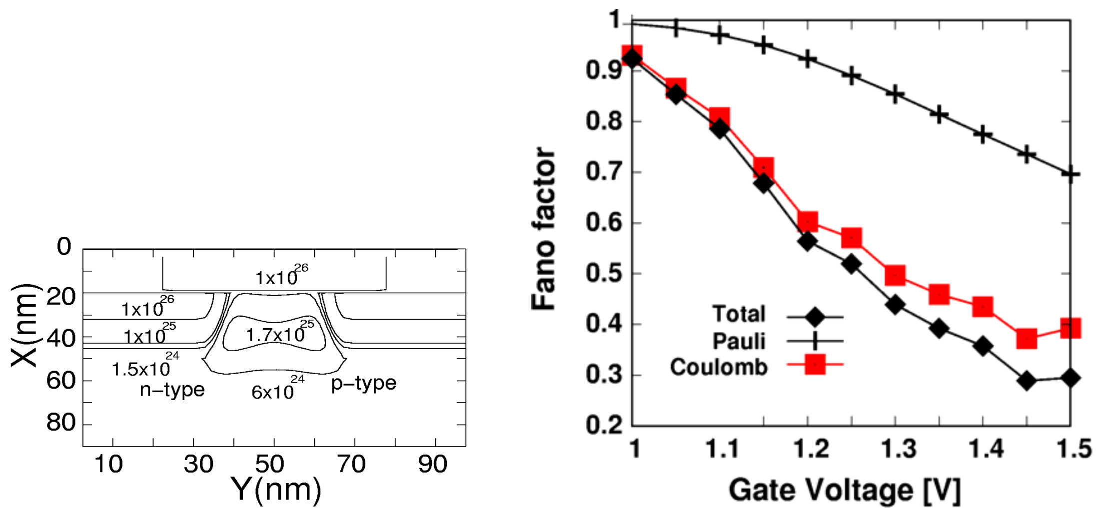

Figure 1: Left: Doping profile of the 25 nm MOSFET considered in the simulation. Right: Fano factor (ratio of the shot noise power to the shot noise power of a Poissonian process) as a function of the gate voltage for drain to source voltage of 1 V. Shot noise is suppressed as a result of both Pauli Exclusion principle and Coulomb interaction.

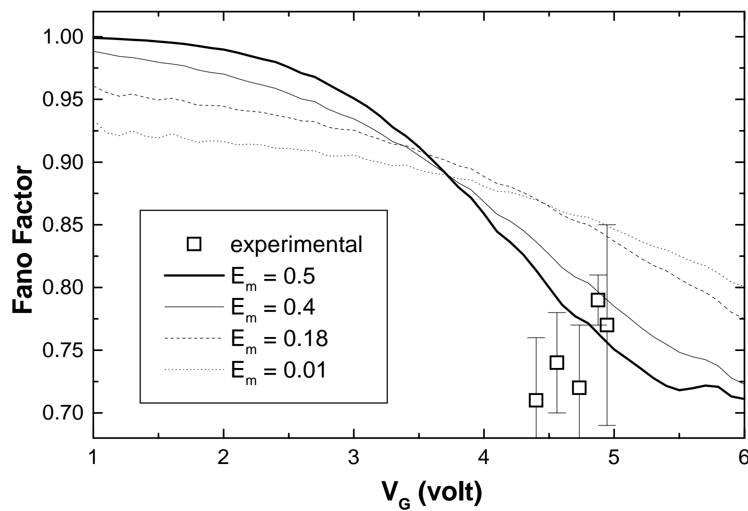

Figure 2: Fano factor as a function of the gate voltage for a MOS capacitor with oxide thickness of 6 nm, in the presence of stress-induced leakage currents, for different energies of the oxide traps with respect to the silicon conduction band. Symbols are experimental values.

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