Simulations of Sub-100nm Strained Si MOSFETs with High-κ Gate Stacks

L. Yang, J. R. Watling, F. Adam-Lema, A. Asenov and J. R. Barker
Device Modelling Group, Department of Electronics and Electrical Engineering,
University of Glasgow, Glasgow G12 8LT, UK
E-mail: L.Yang@elec.gla.ac.uk, Tel: +44 141 330 4792, Fax: +44 141 330 4907

Scaling of Si MOSFETs beyond the 90 nm technology node requires performance boosters in order to sustain the annual increase of intrinsic speed of high-performance [1]. One potential solution is transport enhanced FETs using strained Si channels. High-κ dielectrics required to reduce the gate leakage current for equivalent oxide thickness (EOT) are expected to replace SiO_2 around the 65 nm node in order to enable further scaling. However, achieving high-quality high-κ dielectrics on top of Si is problematic [2]. Aside from these t echnological issues, a fundamental drawback of MOSFETs with high-κ dielectrics is the mobility degradation due to strong soft optical (SO) phonon scattering [3].

In this work we study the impact of interface roughness and soft optical phonon scattering on the performance of conventional and strained Si *n*-MOSFETs with high-κ dielectrics using a self-consistent Ensemble Monte Carlo (EMC) device simulator. The simulated device structures are illustrated in Fig. 1. The test structure for our device simulations are 80nm gate length conventional Si and strained Si (SSi) *n*-MOSFETs with 2.2nm SiO_2 fabricated by IBM [4] and a 35nm gate length *n*-MOSFET with 1.2nm SiON fabricated by Toshiba [5]. The devices with high-κ dielectrics assume the same structures and EOT as the devices with SiO_2. These devices have been carefully analyzed using MEDICI and TAURUS [6] device simulations, to obtain the full device structure, including doping, illustrated in Figs 2 and 3. The simulator includes an unscreened soft optical phonon scattering model [3] and a novel interface roughness (IR) scattering model [7]. The IR has been carefully calibrated with respect to the field dependence mobility behavior and experimental characteristics of the IBM devices [8].

Fig. 4 shows Monte Carlo simulated I_D-V_G characteristics for both the Si and SSi MOSFETs, exhibiting good agreement with the available experimental data [4]. A 35nm Toshiba MOSFET is also simulated, this structure however, is known to have process induced strain in the surface channel, this is represented here to a first approximation as strained Si surface, we find that a 5% Ge content equivalent strain of the channel is appropriate to reproduce the experimental data [5], as shown in Fig. 5. This figure also plots the simulated device characteristics for 35nm devices assuming different amount of strain in the channel and the 35nm device assuming a 20% Ge content equivalent strain, this strain representing the summing of a 15% intentional strain as in the IBM devices, along with a process induced strain. This strained channel delivers ~41% drive current enhancement over the original Toshiba design.

Fig. 6 shows the Monte Carlo simulated I_D-V_G characteristics for an 80nm strained Si MOSFET with a 2.2nm EOT HfO_2. A device current degradation, due to SO phonon scattering form the high-κ, of around 25% at V_G-V_T=1.0V and V_D=1.2V is observed for both conventional and strained Si devices with a 2.2nm EOT HfO_2. Fig. 7 illustrates the Monte Carlo simulated I_D-V_G characteristics for 35nm Si MOSFETs assuming 15% and 20% Ge content equivalent strain with a 1.2nm EOT HfO_2. The drive current degradation due to SO phonon scattering in the 35nm devices is around 8%, which we may attribute to a reduction in SO phonon scattering rate with increasing carrier energy as might be expected at in smaller devices. Our results indicate that the inherent mobility degradation associated with the high-κ gate stack MOSFETs might be compensated for by the introduction of strained Si channels.

---

[1] International Technology Roadmap for Semiconductors (http://public.itrs.net/), 2003
[2] G. D. Wilk, *et al.*, J. Appl. Phys., **89**, p5243, 2001.
[3] M. V. Fischetti, *et al.*, J. Appl. Phys., **90**, p4587, 2001.
[4] K. Rim, *et al.*, Symp. On VLSI Tech., p59, 2001.
[5] S. Inaba, *et al.*, IEEE Trans. Elec. Dev., **49**, p2263, 2002.
[6] http://www.synopsys.com
[7] M. Boriçi, *et al.*, J. Comp. Elec, **2**, p163, 2004.
[8] L. Yang, *et al*, Proc. 5th ULIS, p23, 2004.

A full journal publication of this work will be published in the Journal of Computational Electronics.

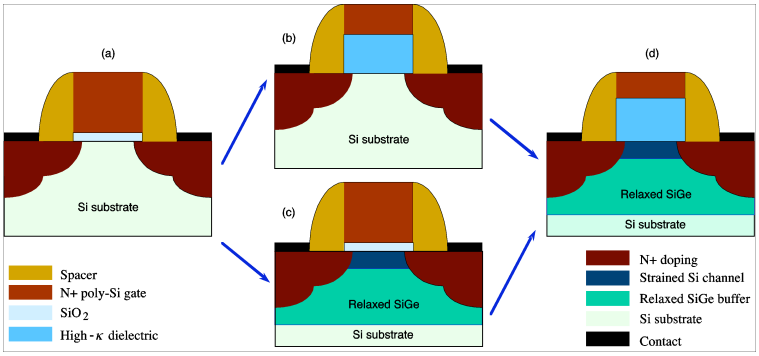

Fig. 1: Simulated device structures: **(a)** conventional bulk Si with SiO_2; **(b)** bulk Si with high-κ dielectric; **(c)** strained Si with SiO_2; **(d)** strained Si with high-κ dielectric

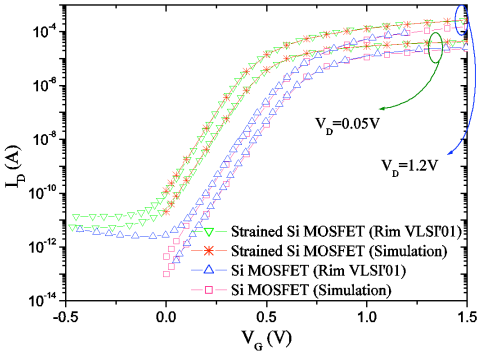

Fig. 2: Calibrated I_D-V_G characteristics of IBM 80nm gate length conventional and strained Si MOSFETs

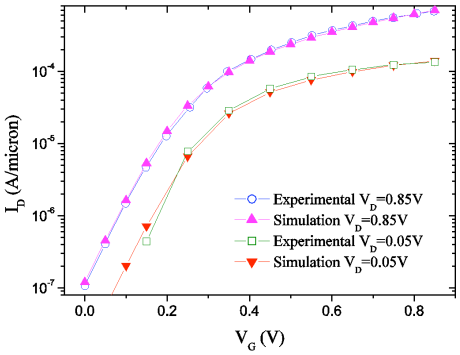

Fig. 3: Calibrated I_D-V_G characteristics of a Toshiba 35nm gate length Si MOSFET

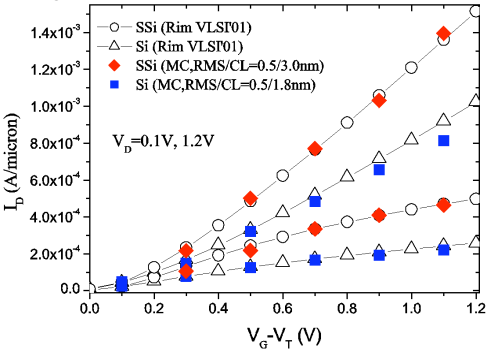

Fig. 4: Monte Carlo simulated I_D-V_G characteristics of 80nm gate length conventional and strained Si MOSFETs

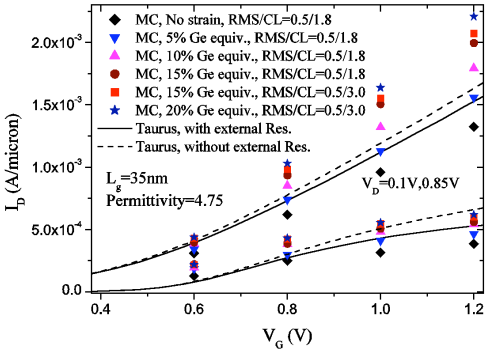

Fig. 5: Monte Carlo simulated I_D-V_G characteristics of 35nm gate length conventional and strained Si MOSFETs

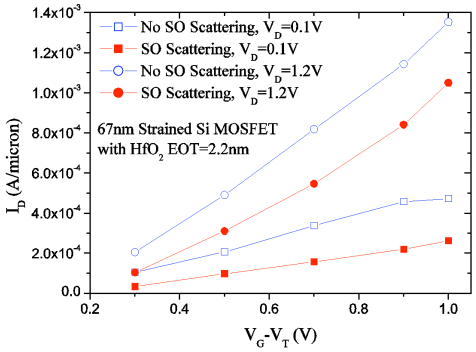

Fig. 6: Monte Carlo simulated I_D-V_G characteristics of 80nm strained Si MOSFETs with HfO_2 (EOT=2.2nm) with and without SO phonon scattering

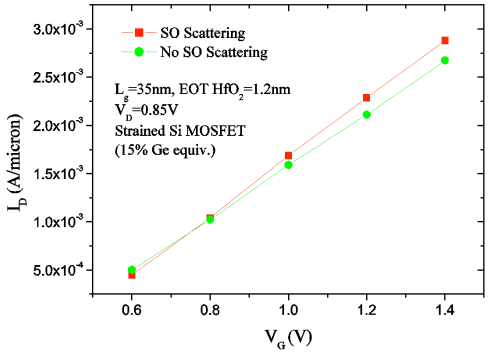

Fig. 7: Monte Carlo simulated I_D-V_G characteristics of 35nm strained Si MOSFETs with HfO_2 (EOT=1.2nm) with and without SO phonon scattering

A full journal publication of this work will be published in the Journal of Computational Electronics.