Arbitrary Crystallographic Orientation in QDAME with Ge 7.5 nm DGFET Examples

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QDAME (Quantum Device Analysis by Modal Evaluation)[1,2] has been extended to permit device simulations with arbitrary orientation between real-space and k-space coordinate systems. We continue to depend on a parabolic, effective mass approximation of the conduction band structure, but now, we can consider any number of E-k ellipsoids with any orientation(s) and energy offset(s) as comprising the conduction band. Note in our two-dimensional self-consistent Poisson-Schrödinger solutions we continue to assume transport is purely ballistic.

Our work resembles in scope the extension of NanoMOS by Rahman, *et al*.[3] to permit arbitrary crystallographic orientation and its subsequent invocation by Low, *et al*.[4] in the context of Ge DGFETs. We differentiate our work from theirs as follows: (i) We solve the two-dimensional Schrödinger equation with appropriately modified traveling wave boundary conditions[5]; no assumptions are invoked concerning the device geometry or the lumping of transport along a centerline of symmetry from source to drain. (ii) We specifically consider 'unusual' crystallographic directions to highlight our simulation capability and to demonstrate that current does not necessarily flow down the center of a symmetric Ge DGFET device structure.

This extension to QDAME involves three areas of program change: (i) Once the relationship between a given ellipsoid's coordinates and the device's coordinates is known, the mixed derivatives generally present in the Hamiltonian are nulled out by a coordinate rotation and change of variables[6]. These new coordinates are then used for analysis. This allows the device's behavior for this energy ellipsoid to be modeled using the existing (diagonal) Hamiltonian discretization. (ii) Traveling wave boundary conditions are reformulated in recognition that the Schrödinger solution changes in the lead regions as well, necessitating a more complicated matching of the wavefunction across the lead-device boundary. (iii) The decomposition of standing waves into traveling waves (unique in our formulation of device transport[1]) must be altered in response to the in-general anisotropic mass present in the lead region. Accordingly, we perform the decomposition along a slanted boundary cutline aligned with the loci of constant wavefunction phase.

Example n-channel 7.5 nm channel length Ge DGFETs will be discussed (see Fig. 1), and the internal device solution details discussed. In particular, our treatment will demonstrate that, in the most general case of crystallographic alignment, current need not flow up the center of an otherwise symmetrical DGFET (see Fig. 2). This result demonstrates the necessity of solving both electrostatics and transport problems in two dimensions in the most general cases.

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A full journal publication of this work will be published in the Journal of Computational Electronics.

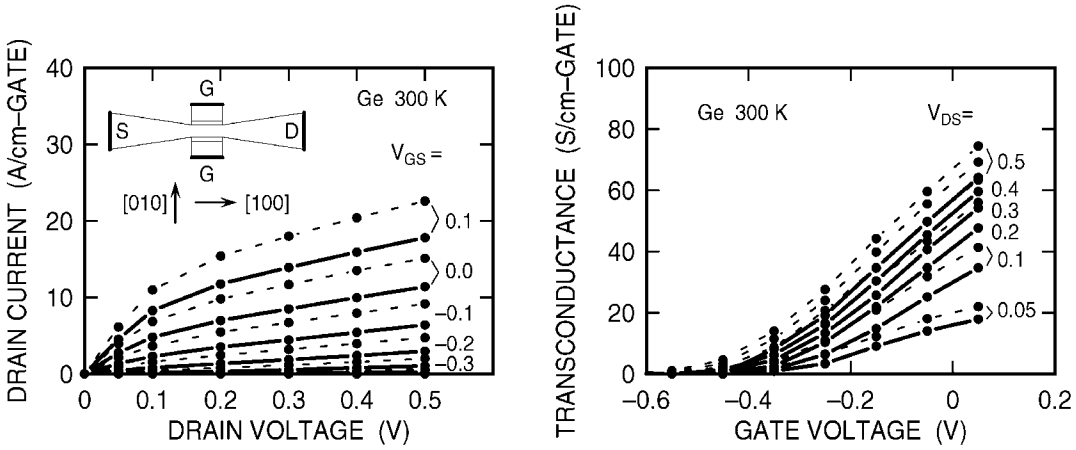

Fig. 1 Output (left) and transconductance (right) characteristics of a Ge DGFET with 7.5 nm channel length and 3 nm channel thickness. Device geometry and crystal alignment are shown in the inset. The solid lines are computed with an eleven valley description (4 L-valleys; 6 X-valleys and 1 Γ-valley); the dotted lines use only the four L-valleys. There is a ~70 mV threshold voltage shift between the two descriptions, but otherwise, very similar behaviors are obtained. Note both ordinates are normalized *per gate*.

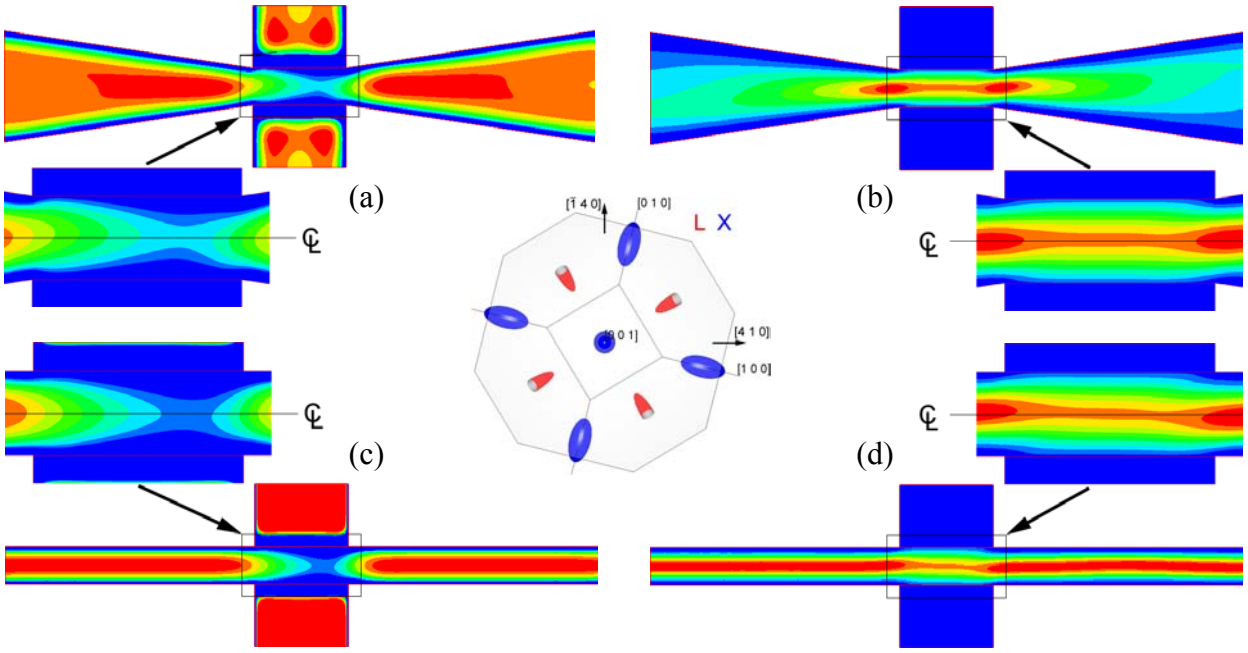

Fig. 2 Electron density (a and c) and current density magnitude (b and d) for a tapered (above) and straight (below) Ge DGFET. The geometries *and* computational meshes are *symmetric* about a horizontal line through the center of the device; however, the solutions are *asymmetric* because of the crystallographic orientation: the horizontal axis is in the [4 1 0] crystal direction; the vertical axis is in the [$\bar{1}$ 4 0] direction. Note the two devices use different gate models (seen in the density: semiconductor above, metal below); asymmetry occurs in both cases for both FET geometries. (Note ℄ denotes the horizontal centerline through the device.)

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