# A Computational Intelligent Optical Proximity Correction for Process Distortion Compensation of Layout Mask in Subwavelength era

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For very large scale integrated (VLSI) circuit and system-on-a-chip (SoC) manufacturing, it requires transferring the desired circuit layouts onto the wafers through lithography processes [1-3]. However, the exposure on wafer has distortions due to the proximity effects [1-3]. As the minimum feature sizes continue to shrink, the mismatch between the desired pattern and the actual result on wafer is no longer ignorable. In the mid-1990s, the progression of smaller feature sizes under Moore's Law approached and eventually crossed the dimensions of the wavelength used for lithography. Since the 180 nm technology node, imaging features smaller than a wavelength would now be routine for all critical layers [1-3]. Hence, a correction of mask patterns between circuit and post exposure result is necessary for obtaining a better agreement. Optical proximity correction (OPC) is the process of modifying the polygons that are drawn by designers to compensate for the non-ideal properties of the lithography process. Given the shapes desired on the wafer, the mask is modified to improve the reproduction of the critical geometry. This is done by dividing polygon edges into small segments and moving the segments around, or by adding additional small polygons to strategic locations in the layout. Various OPC techniques have been developed, which can be grossly grouped into either rule-based or model-based [1-3]. The model-based OPC techniques modify whole layout by the calculations of experimental corrected models [2]. Model-based OPC is capable of more general corrections, but require longer computing time and partition of the simulation domain time to time. Rule-based techniques are an extension of the methods used for manual OPC [3]. They are much fast and therefore may directly apply to an entire layout for semiconductor manufacturing; however they strongly depend on empirical knowledge for an accurate correction.

For rule-based OPC, many additional small polygons are generated by rules to compensate for mask; however we can not decide the size and suitable position of these polygons without any empirical knowledge. In this work, we for the first time develop an intelligent OPC approach which combines the genetic algorithm (GA), the rule-based technique, and conventional model-based correction method to perform the mask correction in subwavelength era. Basic idea is that we apply the GA and the lithography simulator to find out the best size and position for a complete layout with those additional patterns which generated by rules. First of all, an original layout is corrected with rules; the corrected layout is then partition into several sub-domains. For each sub-domain, size and position of those added patterns are optimized with respect to their size and position using the GA algorithm [4]. By solving a two-dimensional Hopkin equation with Fourier transformation, a lithography simulation is performed and the calculated results are used in the calculation of fitness of GA. Depending on the dimension of layout, there are at least hundreds of geometry pattern have to be optimized. This approach accumulates the layout's experience, reduces the requirement of empirical knowledge for performing OPC in layout mask, and effectively achieves the rule-based correction. Fig. 1 shows several simple testing layouts without applied any resolution correction. Fig. 2 shows the corresponding exposed image. It is obvious that there are some distortions between original layout and aerial image in each corner, and this may cause some unexpected mistake in the fabrication of the layout. Figs. 3 and 4 show the OPC corrected layouts and the simulation results of layouts with the proposed intelligent OPC method. This approach can apply to different lithography process, such as the I- and G-line Steppers and DUV.

A computationally intelligent OPC has been proposed for layout mask in subwavelength era. We believe that this methodology benefit the TCAD/ECAD tools and the design and fabrication of VLSI SoC.

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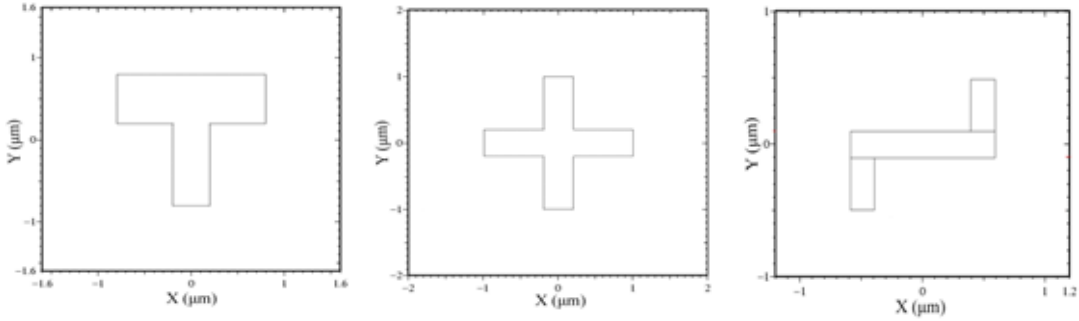


Figure 1: Three testing layout patterns before OPC. The line width of the right figure is equal to 180 nm.

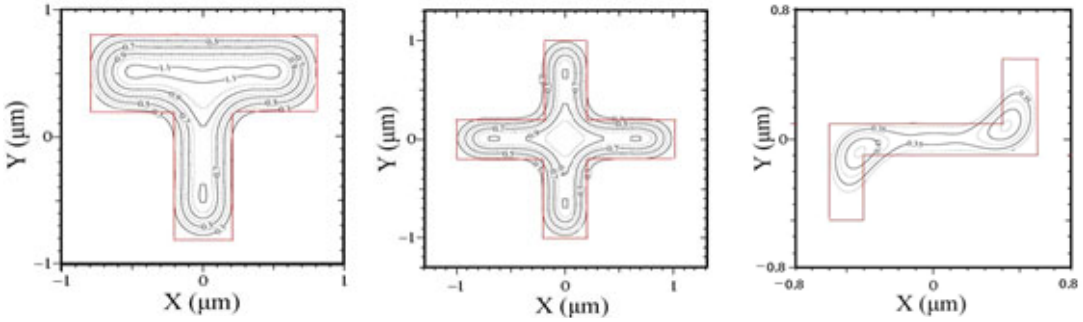


Figure 2: The simulation results of the testing layout patterns of the figure 1. The contour level setting for the interface between two regions is 0.3.

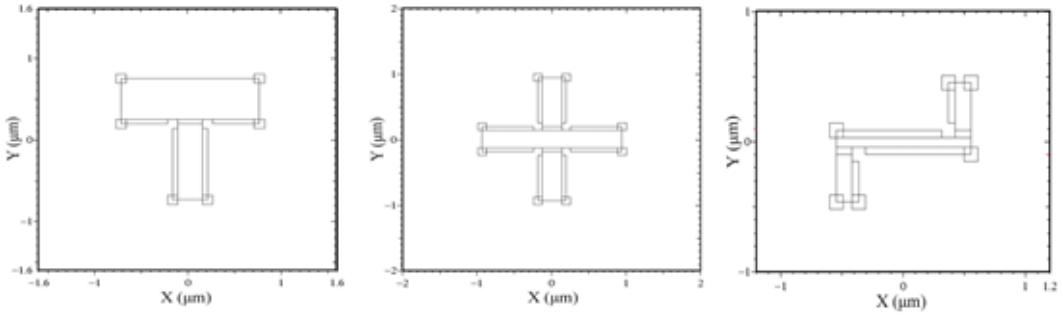


Figure 3: The testing layout patterns after the OPC with proposed method.

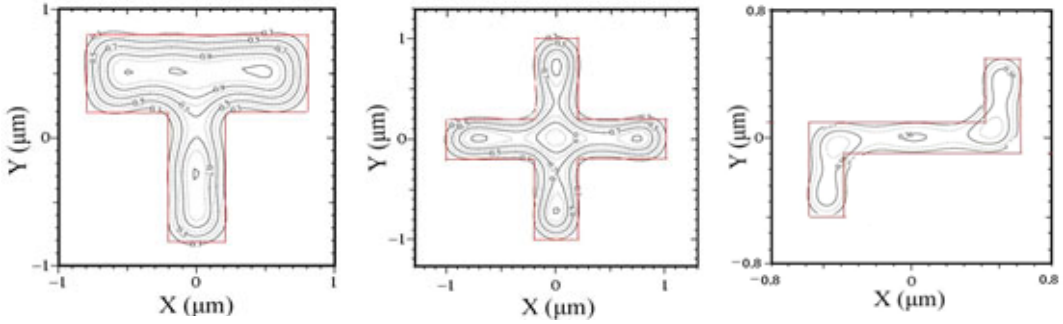


Figure 4: The simulation results of the testing layout patterns after the OPC shown in Fig. 3. Corrections for the corner distortions are found.

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