RTS amplitudes in decanano n-MOSFETs with conventional and high-k gate stacks

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Low frequency (LF) noise in MOSFETs has been a topic of interest to both academia and industry in recent years. It is becoming a major concern for analogue circuit performance, DRAM operation, and will eventually impact critically upon the reliability of digital logic especially as devices continue to scale towards nano dimensions. Random Telegraph Signals (RTS) caused by the capture and emission of carriers in traps at the Si/SiO_2 interface have been posited as a major component of low frequency noise in semiconductor devices. The change in the drain current associated with trapping events in defect states is usually referred to as the RTS amplitude. The magnitude of the RTS amplitude is largest in the subthreshold regime at lower gate voltages and is reduced in the strong inversion regime as mobile charge in the inversion layer increasingly screens out the electrostatic influence of the trapped charge.

In this paper we study the magnitude of the RTS amplitudes in nano-CMOS devices with conventional and high-κ gate stacks. Traps at the front and back gate dielectric interfaces, as well as traps in the body of the dielectric are considered. The impact of poly gate depletion is also taken into account.

Figure 1 presents the dependence of the RTS amplitude on the location of the trapped charge within the channel of a 30×30 nm MOSFET. The RTS amplitude reaches its peak at the centre of the channel where the charge has a strong localised effect on the height of the source-to-drain barrier. When the trapped charge is placed close to the source and drain it has negligible effect on the drain current as the large concentration of mobile carriers in the highly doped source/drain screen out the trapped charge. Figures 2 and 3 illustrate the dependence of the relative RTS amplitude on gate voltage for 30 nm n-channel devices with differing oxide thickness. A single trapped charge is placed in the middle of the channel producing the largest RTS amplitude. For each curve the vertical position of the trapped charge within the oxide is changed, moving from the Si/SiO_2 interface to the gate. As the location of the trapped charge moves towards the gate the electrostatic effect on the channel potential is reduced, hence the RTS amplitude is lower. The thinner oxide in figure 4 has the effect of reducing the magnitude of the RTS amplitudes as the closer proximity of the gate to the channel can more efficiently screen the effect of the trapped charge, smoothing the electrostatic potential within the channel.

Figure 4 presents results for simulations similar to those of figure 3, except that the metal gate has been replaced with a poly-silicon gate. Results for two different poly-silicon gate doping concentrations, 2×10^{19} cm^{-3} and 2×10^{20} cm^{-3}, are shown. With a poly-Si doping of 2×10^{20} cm^{-3} the RTS amplitudes are similar, but slightly higher than those to those for a metal gate. With the lower poly-Si doping the depletion layer at the gate/oxide interface is wider, thus reducing the screening from the mobile electrons in the gate. This leads to higher RTS amplitudes. The simulations presented in figure 4 were repeated for a device with high-κ dielectric (HfO_2) with the same equivalent oxide thickness (EOT = 1 nm) assuming a relative permittivity $\varepsilon_{HfO2} = 22$ and physical oxide thickness $t_{ox} = 5.64$ nm. The results are shown in figure 5. For a trap at the Si/HfO_2 interface (the curves with the highest amplitudes in each case) the results are the same as in the device with SiO_2 gate insulator. However, as the position of the trap gets closer to the gate the reduction in amplitude is more pronounced in the high-κ case.

Figure 6 presents the RTS dependence on trap position in a 30×30nm MOSFET with high-κ dielectric and poly doping $2\times10^{20}cm^{-3}$. Plots corresponding to traps at different levels in the oxide are shown for one quarter of the channel.

A full journal publication of this work will be published in the Journal of Computational Electronics

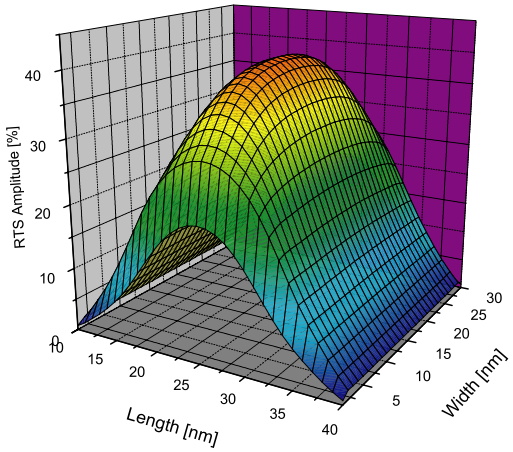

Fig. 1 Dependence on trap position within the channel of RTS fluctuations in the drain current of a 30×30 nm MOSFET.

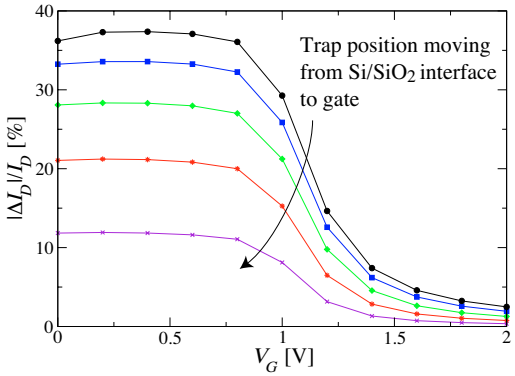

Fig. 2 Relative RTS amplitudes for a 30 nm n–channel MOSFET with t_{ox} = 3 nm and ideal metal gate, for a trap at different positions within the oxide.

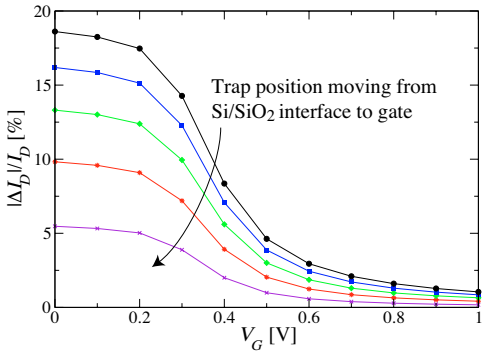

Fig. 3 Relative RTS amplitudes for a 30 nm n–channel MOSFET with oxide thickness, t_{ox} = 1 nm, for a trap at different positions within the oxide. A metal gate is assumed.

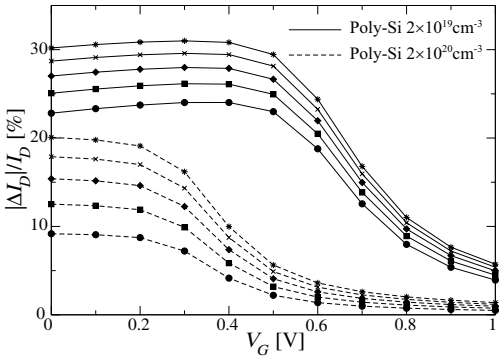

Fig. 4 Relative RTS amplitudes for a 30 nm n–channel MOSFET with t_{ox} = 1 nm, for a trap at different positions within the oxide. Two different dopings of poly-Si gate are shown.

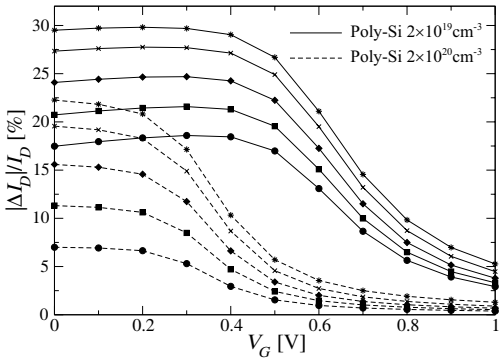

Fig. 5 Relative RTS amplitudes for a 30 nm n–channel MOSFET with high-κ dielectric thickness, t_{ox} = 5.64 nm, for a trap at different positions within the oxide. Two different dopings of poly-Si gate are shown.

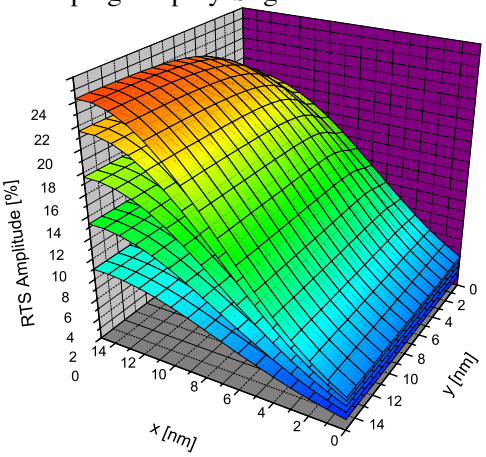

Fig. 6 RTS dependence on trap position in a 30×30 nm MOSFET with high-κ dielectric and poly doping 2×10^{20} cm^{-3}. Plots corresponding to traps at different levels in the oxide are shown for one quarter of the channel.

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