Full-band particle-based analysis of device scaling for 3D tri-gate FETs

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In this work, a 3D tri-gate SOI FET with a wrap around gate geometry is studied using a full-band particle-based simulation tool [3]. Tri-gate FETs show superior scalability over planar device structures, including a reduction of short channel effects [4]. The 3D gate structure of the tri-gate FET not only plays a role in reducing DIBL by shielding the electric field lines from the drain, but also improves gate-channel controllability.

A tri-gate p-FET based on the Omega FET of Yang et al [2] is simulated with a 3D full-band EMC/CMC simulator [3]. The full-band description of the electronic dispersion relation is particularly important for p-channel devices due to the extremely warped shape of the valence bands, even at relatively low energies [5]. The schematic layout of the simulated device and the corresponding potential profile for one bias point is shown in Fig. 1. The potential profile taken along the direction perpendicular to the transport shows the "omega" shape that is characteristic of this tri-gate device geometry [2]. The silicon body thickness, height and width are 25 nm, 50 nm, and 25 nm respectively. The oxide thickness beneath the three gates is 2 nm and the buried oxide is 200 nm.

The device is represented in real-space with a 129 x 65 x 33 inhomogeneous grid. This large number of grid cells is required to resolve the high doping density and, as a result of the highly inhomogeneous cells, a huge number of simulated particles (> 200,000) is required to represent the hole population. Typical simulations take approximately 48 CPU hours to simulate 1 ps. The hole velocity and energy averaged along the entire silicon body is shown in Fig. 2 along the direction of current flux. As can be seen, the average hole velocity in the channel is greater than the saturation velocity (~ 7 x 10^6 cm/s). In Fig. 3, the current-voltage characteristics are presented and demonstrate good saturation and transconductance. The approximate values of the transconductance and channel conductance obtained from the simulation are 1800 μS/μm and 1000 μS/μm, respectively. Considering the absence of information available concerning the impurity profiles and contact resistance, these values compare well to the experimental ones.

In this work the impact of scaling the thickness, width and height of the tri-gate p-FET is investigated. In particular, the role of scaling each of these characteristic dimensions on the short-channel and short-width effects (such as DIBL and sub threshold swing) is examined. An analysis of the frequency response of the tri-gate structure is also performed to investigate the influence scaling has on the dynamic response. Since impact ionization is an important mechanism in these scaled devices due to the high internal electric fields, the role of impact ionization is also investigated [5].

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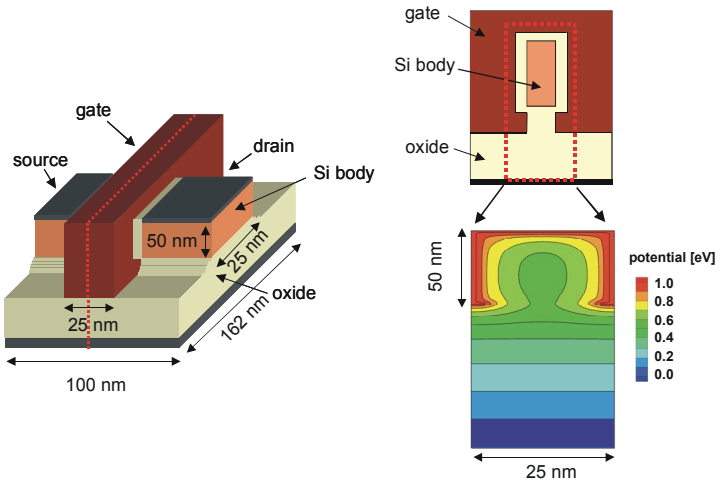

Figure 1: Schematic layout of the 3D tri-gate FET and the corresponding potential cross-section in the region designated by the dashed square.

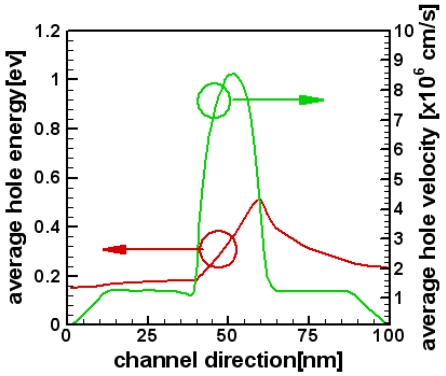

Figure 2: Hole energy and velocity in the direction of transport from source to drain, both averaged over the entire silicon body of the p-FET with V_g = -1.55 V and V_d = -1.0 V.

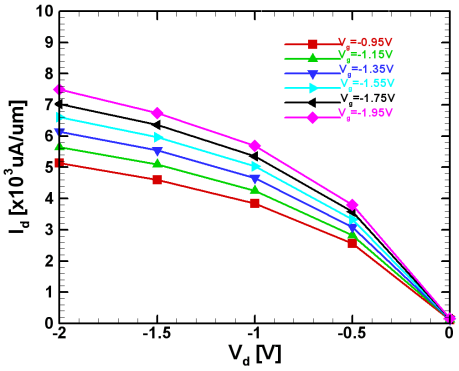

Figure 3: Current - voltage curves for the 25 nm tri-gate SOI p-FET with $|V_g|$ step= 0.2V