3D Monte Carlo simulation of FinFET using FMM algorithm

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Conventional bulk MOSFETs will eventually fail as devices are scaled down toward nanoscale regime due to severe short channel and tunneling effects. Because of these issues, fully-depleted double-gate (DG) MOSFETs emerge as a solution for next generation nanoelectronic devices. Among different DG devices, FinFETs have evolved as the most promising candidate because of their good immunity to short channel effects. In such devices, quantum effects start dominating the device performance due to ultra short dimensions so that simple analytical models should be replaced by comprehensive approaches.

We use 3D Monte Carlo device simulator with non-parabolic band-structure in conjunction with the novel *effective potential* scheme [1] for treatment of quantization effects. Moreover the recently proposed FMM algorithm [2] for fast and efficient calculation of Coulomb interaction is included. Our experience shows that the use of FMM algorithm along with the Monte Carlo transport kernel can give us about a factor of 10 reduction of the CPU time. This is a consequence of the fact that in normal 3D Monte Carlo – 3D Poisson equation solvers, about 90% of the simulation time is spent in consecutive solutions of the 3D Poisson equation, irrespective of the type of solver used (Bi-CGStab or multi-grid). When FMM method is utilized in conjunction with the 3D Monte Carlo simulator, Poisson equation is solved only once at the beginning to account for the boundary conditions. Therefore, significant speed-up of the computations is achieved.

FinFET devices have been simulated with S/D doping of 10^{19} /cm^3 and fin doping of 10^{16} /cm^3. The relative position of the gate with respect to S/D, called fin extension, plays a significant role in controlling the device performance. Effect of equal and unequal fin extension has been investigated. n^+ polysilicon gate has been assumed as a metal electrode. For n-channel FinFET, shown in Figure 1, the threshold voltage can be made positive by adjusting metal-gate work-function approximately equal to the mid bandgap of silicon. The average carrier drift velocity and the average carrier energy are plotted on the left and right panels of Figure 2, respectively. The device transfer and output characteristics for a set of gate and drain biases are shown in the left and right panel of Figure 3. It is important to note that the amount of velocity overshoot that one observes in this device structure depends upon the choice of the fin dimensions and the contact material used (different metals or heavily-doped poly-silicon).

Another issue under investigation is the role of unintentional doping on the device performance. Our initial suggestions on similar types of structures suggest about 20-40% decrease of the on-state current when a single impurity atom sits at the source end of the channel region [3]. Therefore, due to the small width of the FinFETs, we believe that unintentional doping, i.e. the presence of even a single impurity in the active channel region of this device, might play significant role when compared to narrow-width SOI devices.

1. D. K. Ferry, R. Akis, and D. Vasileska, "Quantum Effects in MOSFETs: Use of an Effective Potential in 3D Monte Carlo Simulation of Ultra-Short Channel Devices", *IEDM Tech. Dig.*, pp. 287-290, 2000.
2. L. Greengard and V. Rokhlin, "A fast algorithm for particle simulations," *J. Com. Phys.*, vol. 135, no. 2, pp. 280–292, 1997.
3. S. Ahmed and Dragica Vasileska, "Modelling of narrow-width SOI devices", *Semi. Sci. and Tech.*, vol. 19, pp. 131-133, 2004.

A full journal publication of this work will be published in the Journal of Computational Electronics.

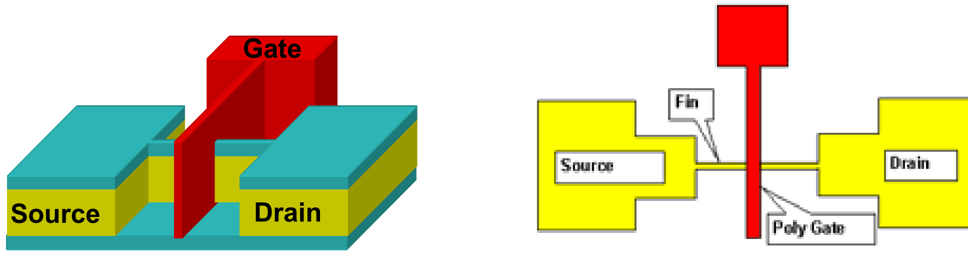

Figure 1. Schematic view of the structure being simulated. Left panel – side view, right panel – top view.

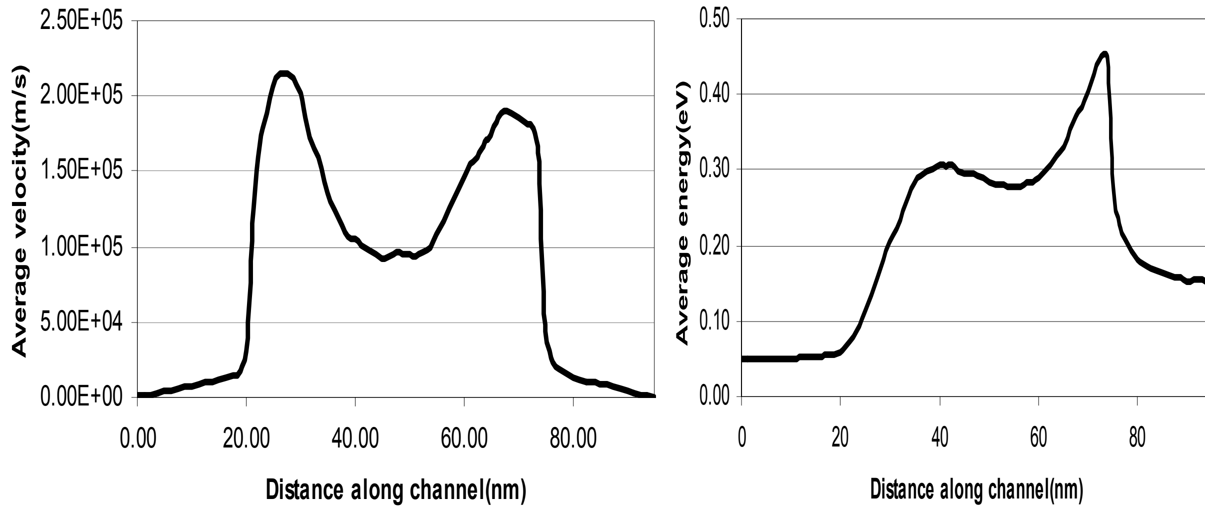

Figure 2. Left panel – average carrier velocity, right panel – average carrier energy. The applied bias is $V_G = 1$ V and $V_D = 1$ V.S/G gap=15nm, D/G gap=20nm

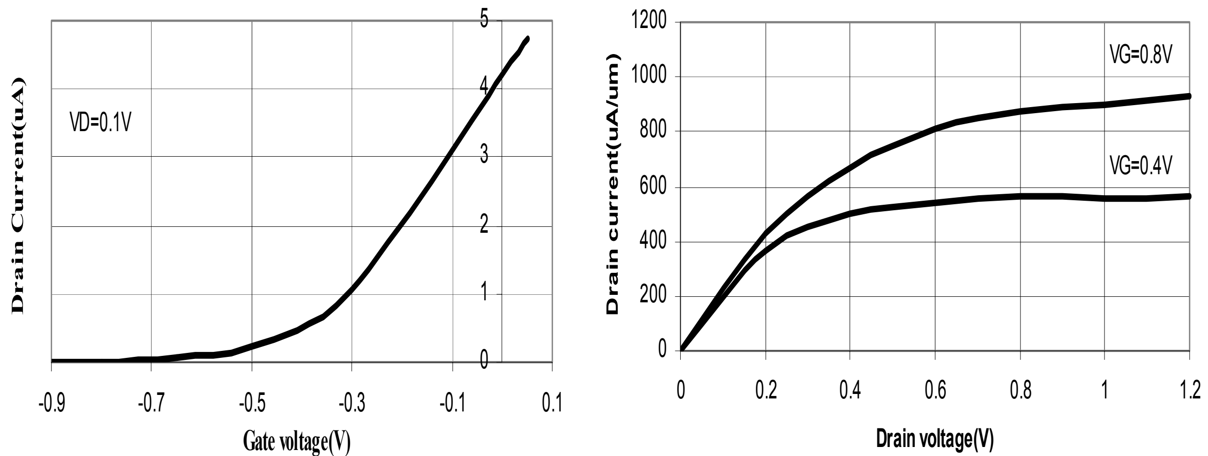

Figure 3. Left panel – device transfer characteristics. Right panel – output characteristics for two values of the gate voltage. S/G gap=15nm, D/G gap=15nm. Notice the slow turn-on of the device which means further device optimization is needed.

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