Monte Carlo simulation of electron velocity overshoot in DGSOI MOSFETs

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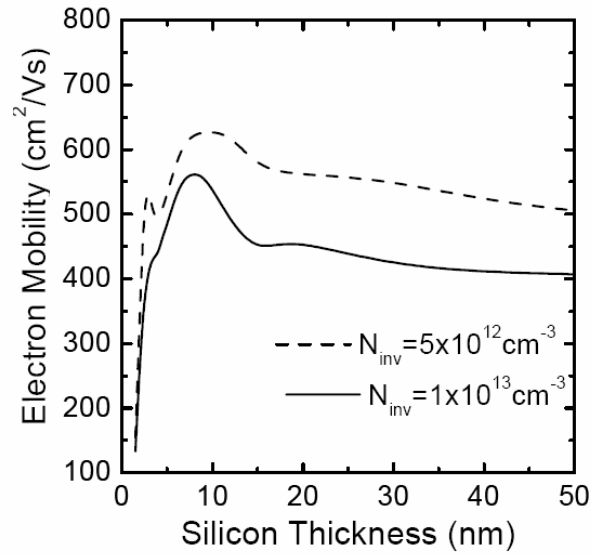
Velocity overshoot (VO) is one of the most important new effects observed in very short channel Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), as this is directly related to the increase in current drive and transconductance experimentally observed. Some authors have shown that experimental measurements of submicron MOSFET transconductances are higher than the theoretical maximum transconductance that can be reached in the case where electrons drift in equilibrium with the lattice, their electron velocity being limited by the saturation velocity. This fact implies that if velocity overshoot could be controlled, the performance of very short-channel MOSFETs would be improved much more than previously expected with respect to the performance of long-channel transistors, not only because the transit time is reduced due to a shorter channel length but also because the drift velocity along the channel is higher than the saturation velocity.

Double Gate MOSFETs are considered serious alternatives to conventional MOSFETs in deep submicron device electronics because of the advantages they show in connection with the reduction of the parasitic capacitances, short channel effects, increased radiation tolerance and increased mobility (due to volume inversion), etc. In addition, like other dual gated devices, DGMOSFETs are claimed to be more resistant to short channel effects (SCE) than are bulk silicon MOSFETs and even than single gate fully depleted SOI MOSFETs. This is due to the fact that the two gate electrodes jointly control the carriers, thus screening the drain field away from the channel. This characteristic would permit a much greater scaling down of these devices than for conventional MOSFETs. As a consequence, VO effects are extremely important in these devices because their advantages make them capable of severe channel length reductions.

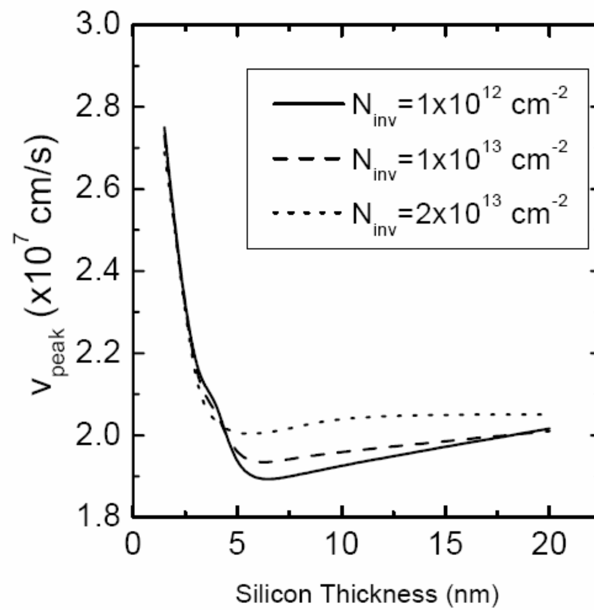
Taking into account the comments above, we have performed a comprehensive study of velocity overshoot effects in double gate MOSFETs. A Monte Carlo simulator coupled with a self-consistent Poisson-Schroedinger solver was used to calculate velocity overshoot effects, low field mobilities, average conduction effective mass, and wavefunction overlapping.

It is shown that higher velocity overshoot effects are obtained at lower inversion charges and smaller silicon layer thicknesses. In general, electron transport properties in DGSOI MOSFETs are governed by two opposite effects as the silicon thickness decreases: the reduction in the average conduction effective mass and the increase in the phonon scattering rate. However, we have seen that for very thin silicon thicknesses (T_{Si}<5nm) while electron mobility is mainly limited by the phonon scattering rate, and therefore abruptly falls as T_{Si} decreases, the velocity overshoot peak is mainly determined by the average conduction effective mass, such that highest VO values are achieved for the smallest silicon thicknesses, where the minimum values of the conduction effective mass (and the highest phonon scattering rates) are obtained. In ultrashort channel length devices, where velocity overshoot dominates the electron transport through the channel, the best performance is obtained as the silicon thickness is reduced below 5nm. However, from the point of view of electron mobility, silicon thicknesses ranging from 5nm to 10nm are preferred. In conclusion, velocity overshoot enables further reduction in the device channel length, in contrast to what might be supposed from the low-field mobility behavior.

A full journal publication of this work will be published in the Journal of Computational Electronics .



(a)



(b)

Figure 1: (a) Evolution of low-field electron mobility for a DGSOI inversion layer with the thicknesses of the silicon layer. Two different values of inversion charge concentration are considered. Phonon and surface-roughness scattering are taken into account. (b) Evolution of velocity overshoot peak for a DGSOI inversion layer with the thickness of the silicon layer for different values of inversion charge concentration.

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