Search for Optimum and Scalable COSMOS*

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The Si nanoelectronic engineering have recently reached a level of capability, which make 3D processing on silicon-on-insulator (SOI) substrates not only possible [1,2], but also a necessity in order to surmount practical limitations of conventional planar CMOS [3]. Thus, device modelers are presented with a multitude of options in exploring new designs, as evident in the proliferation of alternative architectures, including multi-gate MOSFETs, Schottky MOSFET and Tunneling MOSFET. While these structures have unique features superior to conventional MOSFETs, nonetheless, they all aim to replace the bulk devices in traditional CMOS circuitry. In other words, they still retain the redundancy inherent to CMOS operation, namely building two devices even though only one operates at a given stable output.

We have recently demonstrated [4], through the use of device simulations, that a symmetrically operating CMOS device pair may be built under a *single gate structure* by a surprisingly simple choice of device layout and channel engineering parameters. The new architecture, named *complementary orthogonally stacked* MOS (COSMOS*), places the n and p MOSFETs perpendicular to one another under a single gate, integrating them vertically (see Fig.1&2). Thus COSMOS can eliminate the aforementioned redundancy in CMOS and result in dramatic savings (>50%) in device active area of a conventional *digital* CMOS layout, but also reductions in R·C device parasitics associated with building and wiring two sets of devices for a single Boolean output function.

The proposed COSMOS architecture relies for operation on several important modifications. Firstly, a conventional silicon electron channel must be grown atop a strained SiGe hole channel, as shown in Fig.2. To facilitate threshold tuning, reduce parallel conduction and eliminate need for doping, Ge concentration in the strained channel must be high. In accordance, the gate material may be a mid-gap metal, poly-SiGe alloy or polySi, depending on the choice of Ge concentration or background doping. Moreover, we also propose the channel layers to be grow or bonded [5] on a SOI substrate to easily isolate n and p MOSFETs, while also keeping with the general scaling trends associated with a low-leakage and low-parasitic SOI substrate. For an example layer structure with a 4nm strained-$Si_{0.3}Ge_{0.7}$ hole channel and 3nm Si electron channel under a mid-gap metal gate, 1D self-consistent Poisson-Schrödinger simulation of this structure (see Fig.3) indicate that symmetric population of both channels is possible with a threshold of V_T=±0.2-0.4 V. We also find that there is no significant parallel conduction in this layer structure, removing concerns for isolation in the stacked channels under bias.

It must be noted that respective carriers in the channels of COSMOS layers are well confined and carrier densities are comparable, as shown in Fig.4&5. Furthermore, the use of large Ge concentration in the *buried* strained channel should improve hole mobility considerably over that of electrons in Si inversion channel. Thus, for x=0.7, hole mobility in starined $Si_{1-x}Ge_x$ layers should be comparable to or larger than electron mobility in undoped Si inversion layer. By aligning pMOSFET along the [011] direction [6], hole mobility may be further improved, thus restoring pMOSFET transconductance deficit due to larger seperation from the gate. Thus, there are several independent parameters of layer structure, including layer composition, thickness and order, which can be used to optimize a symmetric COSMOS device threshold.

A basic concern for vertically integrating two devices would be the isolation of parasitic p-i-n diodes, which may turn on inadvertently. To prevent this in real devices, additional etching steps are needed during the construction of COSMOS structure. We show in Fig.6, how a simple COSMOS inverter (NOT gate) may be built using selective wet-etch processes [7]. Note that the strained SiGe layer must be partially etched underneath the top Si layer. To complete the inverter, a *short* metallization layer is sufficient, hence reducing total RC losses considerably. In Fig.7 we provide verification of the COSMOS inverter operation using 3D TCAD simulations based on drift-diffusion approximation. Clearly, the inverter is operational and is especially suitable for low-power applications due to static leakage from p-i-n parasitic diode at high drive conditions.

In the present work, we report the result of 3D simulations aimed at optimizing structural parameters for tuning symmetric operation of COSMOS, improving leakage and switching performance. In addition, we also investigate the scalibility of COSMOS structure as a function of lateral and vertical device dimensions. Thus we will show how significant area gains can be obtained in static CMOS logic circuits, where the built-in orthogonality of the COSMOS should be most beneficial.

* Patent pending.

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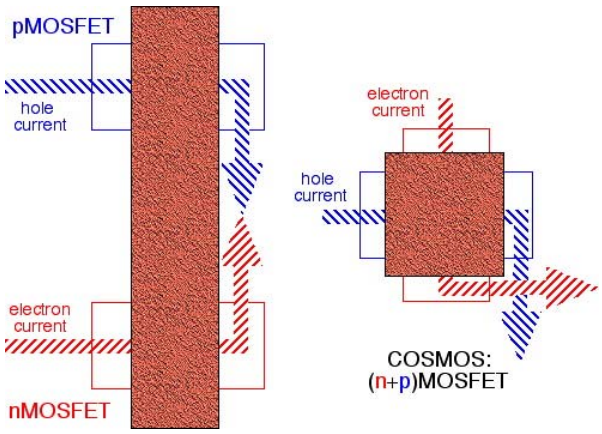

FIGURE 1: Current paths for n or p MOSFETa in conventional CMOS and proposed COSMOS architecture. A significant reduction in active area and device parasitics is obtained in the latter case.

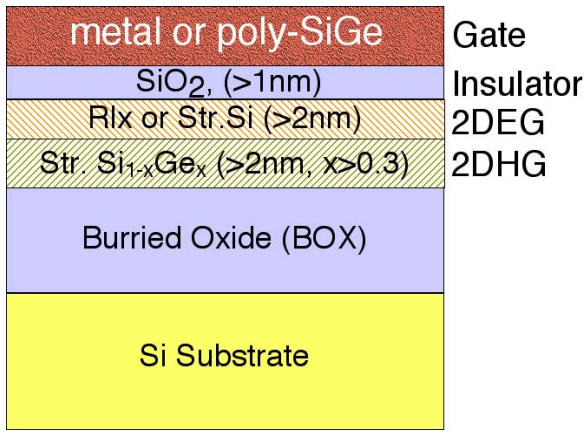

FIGURE 2: A typical layer structure (x=0.7) needed for successful integration and symmetric operation of COSMOS devices. Alternative designs is possible by varying gate material or x.

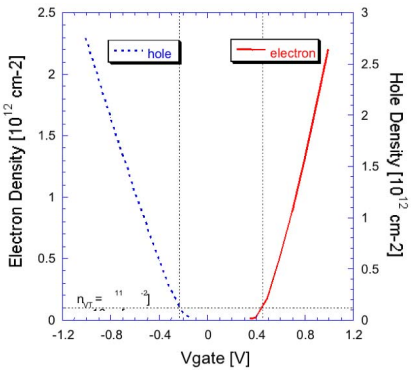

FIGURE 3: Carrier density against gate voltage in layer design in Fig.2. x=0..7 and Φ_m=4.67eV. Note that (a)symmetrical operation ($|V_T|\approx 0.3\pm 0.2$) is possible with a suitable choice of parameters x and Φ_m.

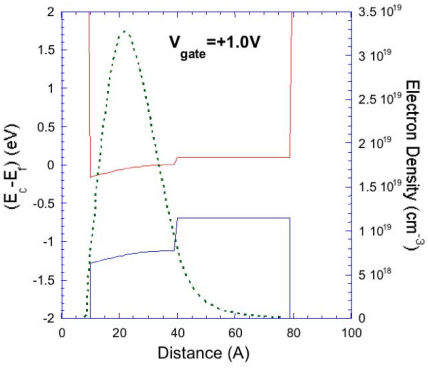

FIGURE 4: 1D electron distribution and band diagram under the gate for a bias voltage of +1.0V. No parallel channel exists and electron distribution peaks near the insulator interface, reducing mobility that of bulk.

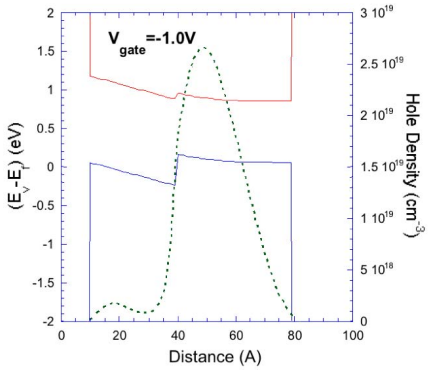

FIGURE 5: 1D hole distribution and band diagram under the gate for a bias voltage of -1.0V. Hole density peaks at the canter and should not suffer from interface roughness or parasitic channel effects.

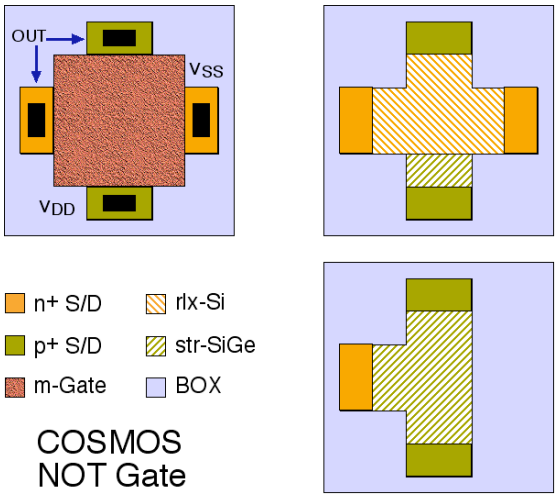

FIGURE 6: Top view of the proposed COSMOS inverter, with appropriate connections. Peeled-off view of the COSMOS pair isolated using two selective etch steps are explained on the right: upper right without the gate and insulation layer, and lower right without the intermediate relaxed-Si layer.

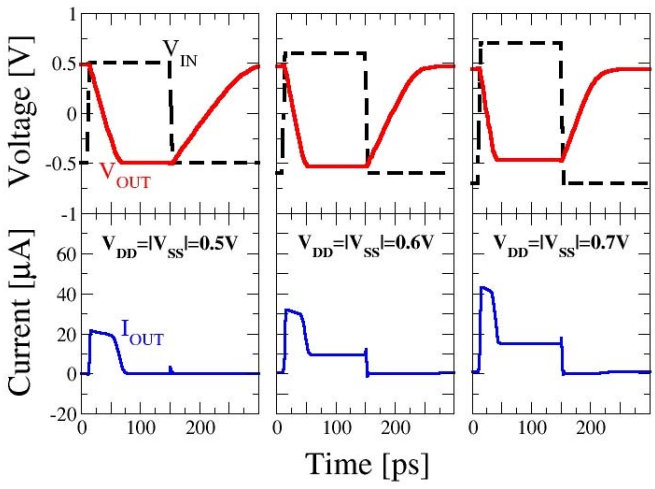

FIGURE 7: Demonstration of transient response of COSMOS inverter driven at different rail voltages (digital levels). Note that for ±0.5V drive the device operates successfully with a ~150ps average delay and no appreciable loss in noise margin that we see happen at higher drive voltages as a result of static leakage

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